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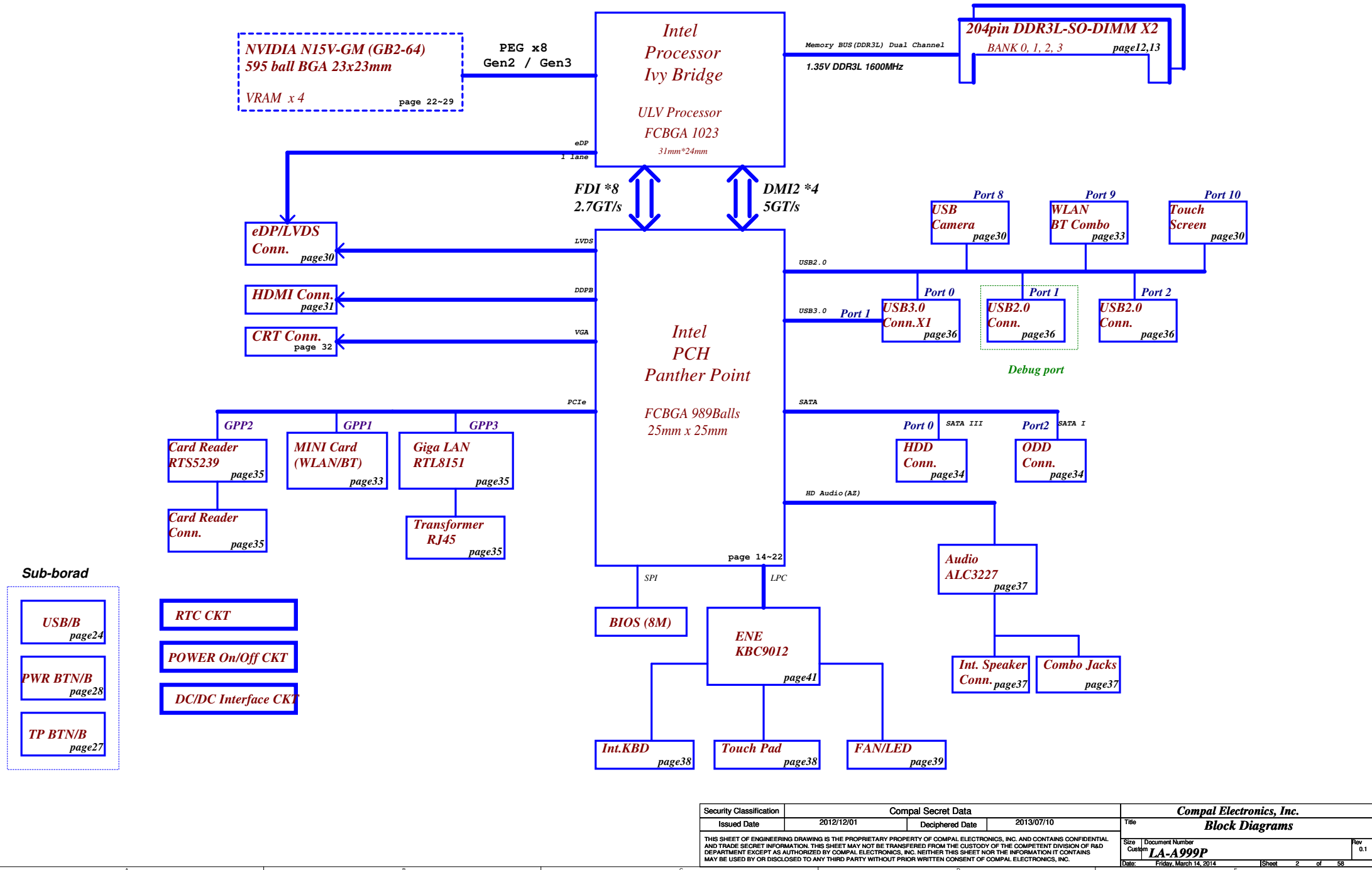
SLC M/B Schematics Document

14": Tabo; 15.6" Pochacco

Intel Ivy Bridge ULV Processor with DDRIII + Panther Point

Date : 2013/11/13
Version 0.1

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	Block Diagrams
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ZSO40/50 (LA-A998P/LA-A999 Ver:0.1)

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
		ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.675VS	+0.675VP to +0.675VS switched power rail for DDR3L terminator	ON	OFF	OFF
+1.05VS_VCCP	+V1.05SP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+VCCP	+VCCP (1.05V) power for PCH	ON	OFF	OFF
+1.35V	+1.35V_VDDQP to +1.35V power rail for DDR3L	ON	ON	OFF
+1.5VS	+1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+3VALW) to 1.8V LDO power rail to PCH	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VL to KBC	ON	ON	ON*
+LAN_VDD_3V3	+3VALW to +LAN_VDD_3V3 power rail for LAN	ON	ON	ON*
+3V_PCH	+3VALW to +3V_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V_PCH	+5VALW to +5V_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Power Plane	Description	S1	S3	S5
+3VGS	GPU power	PX	OFF	OFF
+VGA_CORE	GPU power	PX	OFF	OFF
+1.05VGS	GPU power	PX	OFF	OFF
+1.5VGS	GPU power	PX	OFF	OFF

EC SM Bus1 address

Device	Address
Smart Battery	
G-sensor	0x50/0x52
Charger IC BQ24738	0xFFH

EC SM Bus2 address

Device	Address
PCH SML1	
N15V-GE dGPU	

PCH SM Bus address

Device	Address
DDR DIMM0	
DDR DIMM1	

SMBUS Control Table

	SOURCE	BATT	WLAN MIIN1	BATT Charger	TP	SODIMM	EC_SMB_CK2 EC_SMB_DA2	PCH_SML1CLK PCH_SML1DATA	G-Sensor	dGPU	
EC_SMB_CK1 EC_SMB_DA1	KB9012	V		V					V		
EC_SMB_CK2 EC_SMB_DA2	KB9012							V		V	
PCH_SMBCLK PCH_SMBDATA	PCH					V					
PCH_SML0CLK PCH_SML0DATA	PCH										
PCH_SML1CLK PCH_SML1DATA	PCH						V				

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	mini WLAN	CLKOUTFLEX0	None
			CLKOUTFLEX1	None
	CLKOUT_PCIE1	CARD READER	CLKOUTFLEX2	None
	CLKOUT_PCIE2	PCIE LAN	CLKOUTFLEX3	DGPU_PRSNT#
	CLKOUT_PCIE3	None		
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		



Symbol Note : means Digital Ground



: means Analog Ground

Project ID	UMA@	DIS@		
------------	------	------	--	--

PCB	LA-A998P	LA-A999P
	14@	15@

BY SKU		
TPM	9635@	9656@
CPU	CPUUMA1@ CPUUMA2@ CPUDIS@	
VRAM	X76@ MIC@	SAM@ HY@

Option	@	CONN@	SP@	PX@	UMA@	DIS@	
UMA	X	X	V	X	V	X	
DIS	X	X	V	V	X	V	

CLKOUT	DESTINATION
PCI0	PCH_LPBACK
PCI1	PCI_LPC/TPM
PCI2	None
PCI3	None
PCI4	None

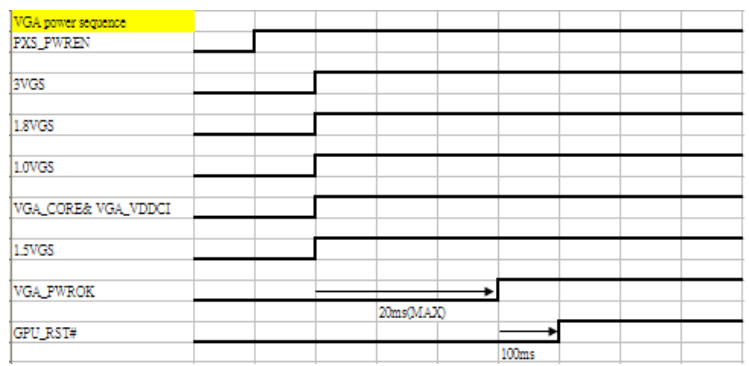
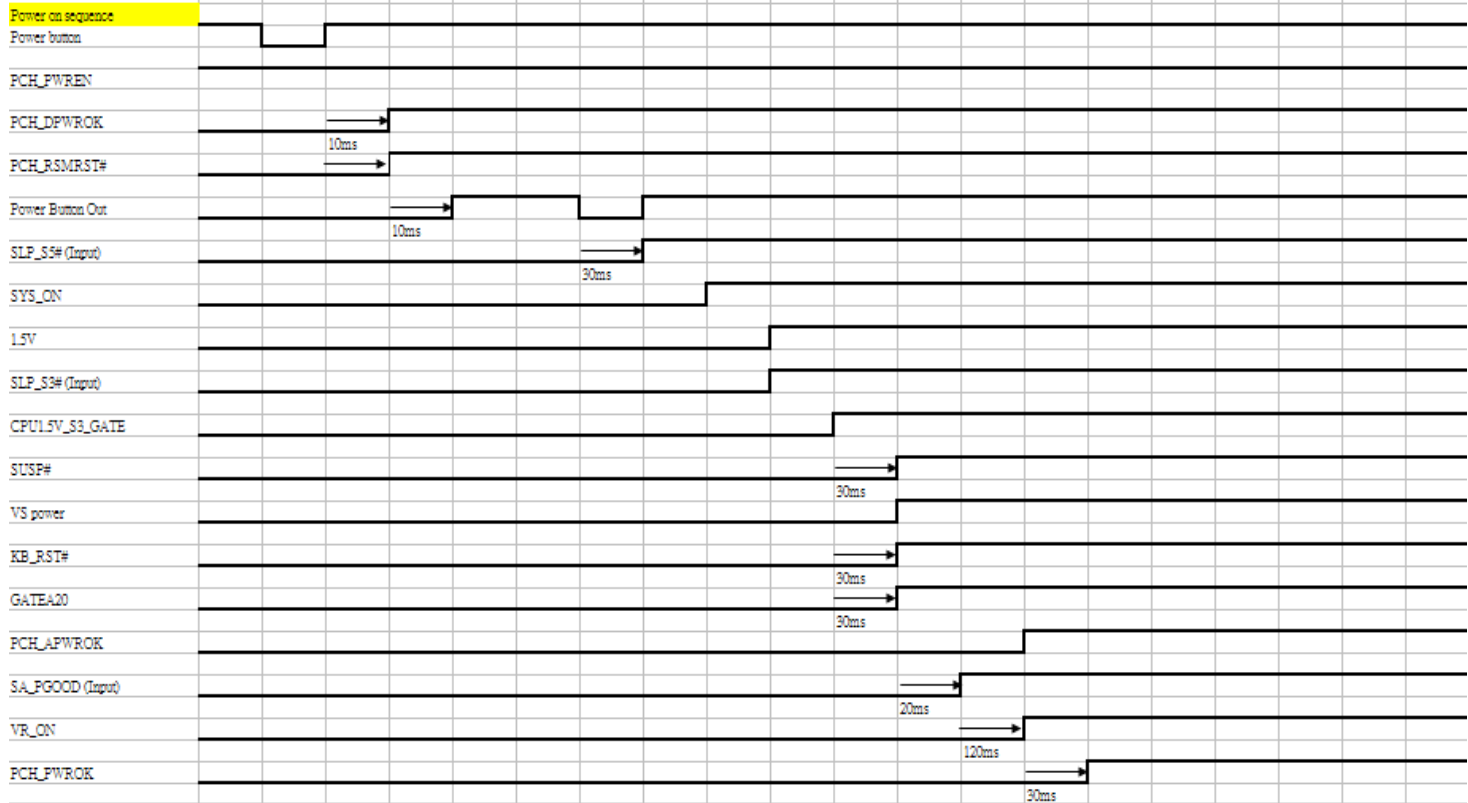
SATA	DESTINATION
SATA0	JHDD1
SATA1	None
SATA2	JODD1
SATA3	None
SATA4	None
SATA5	None

USB Port Table

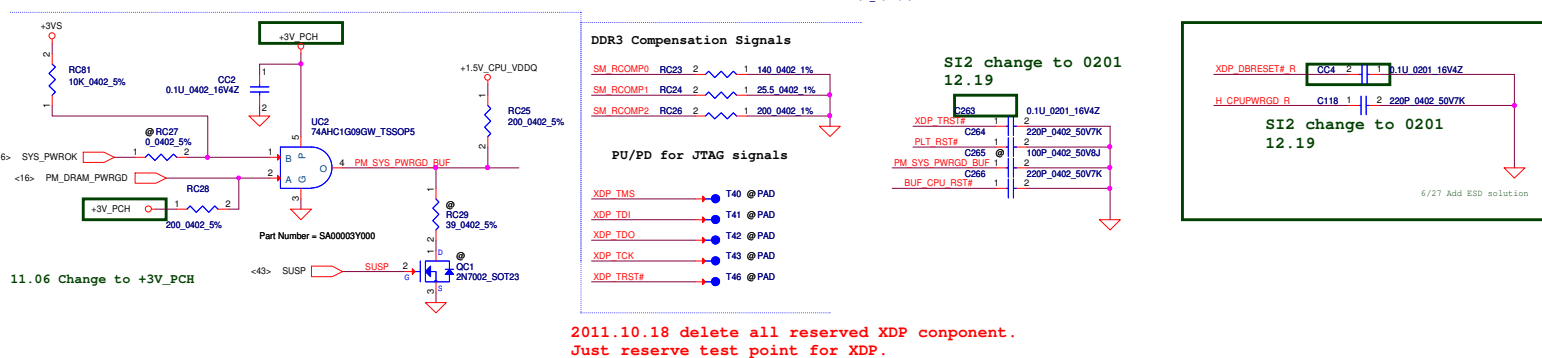
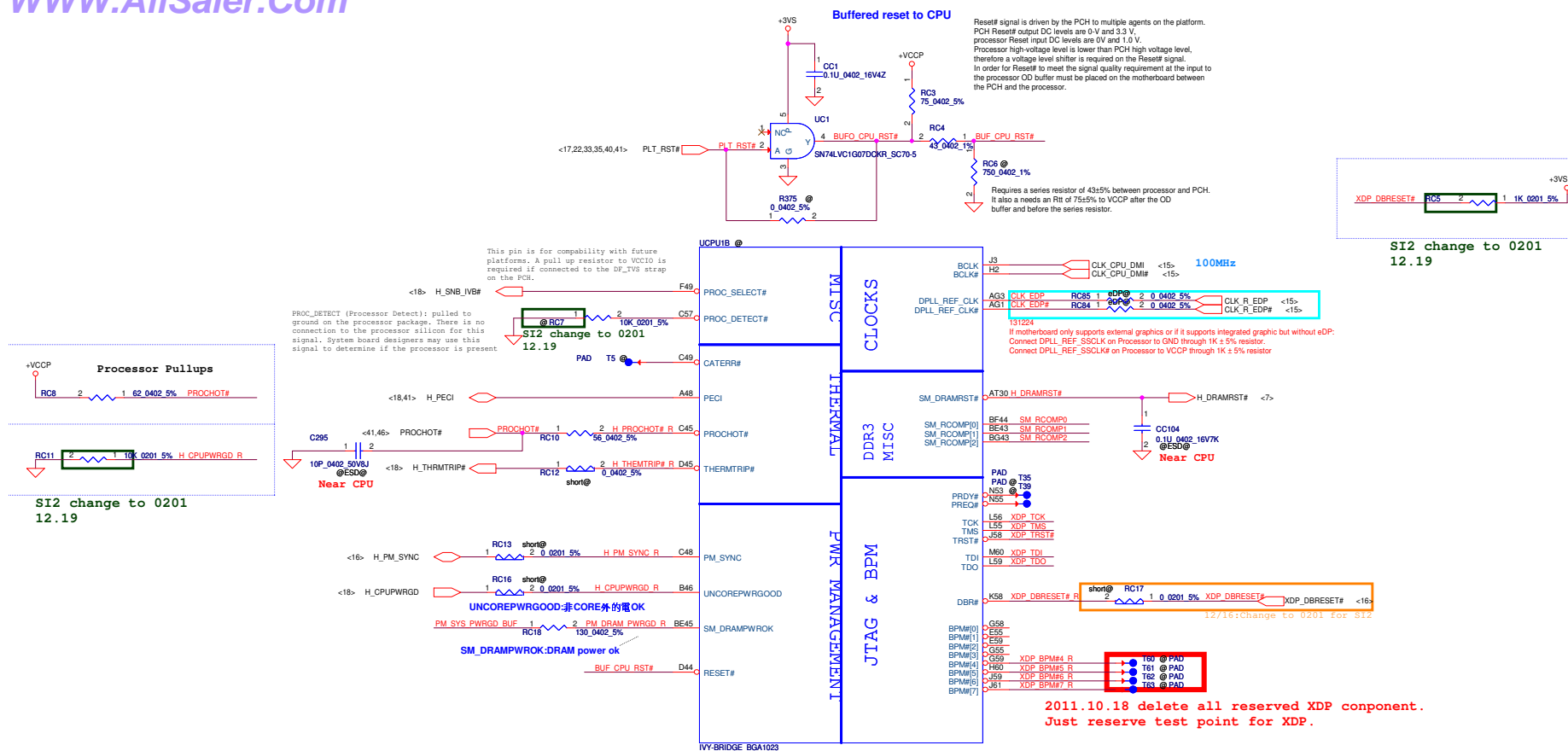
USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB2.0 (For USB3.0 Conn.)
		1	USB2.0 (D/B)
	UHCI1	2	USB2.0 (D/B)
		3	None
	UHCI2	4	None
		5	None
EHCI2	UHCI3	6	None
		7	None
	UHCI4	8	Camera
		9	Mini Card(WLAN& BT)
	UHCI5	10	Touch Screen
		11	None
	UHCI6	12	None
		13	None

USB 3.0	Port	2 External USB Port
	1	USB3.0 (left Side)
	2	None
	3	None
	4	None

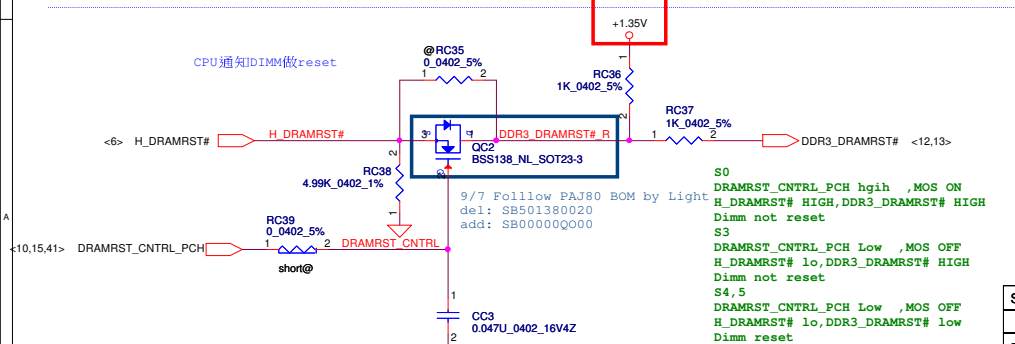
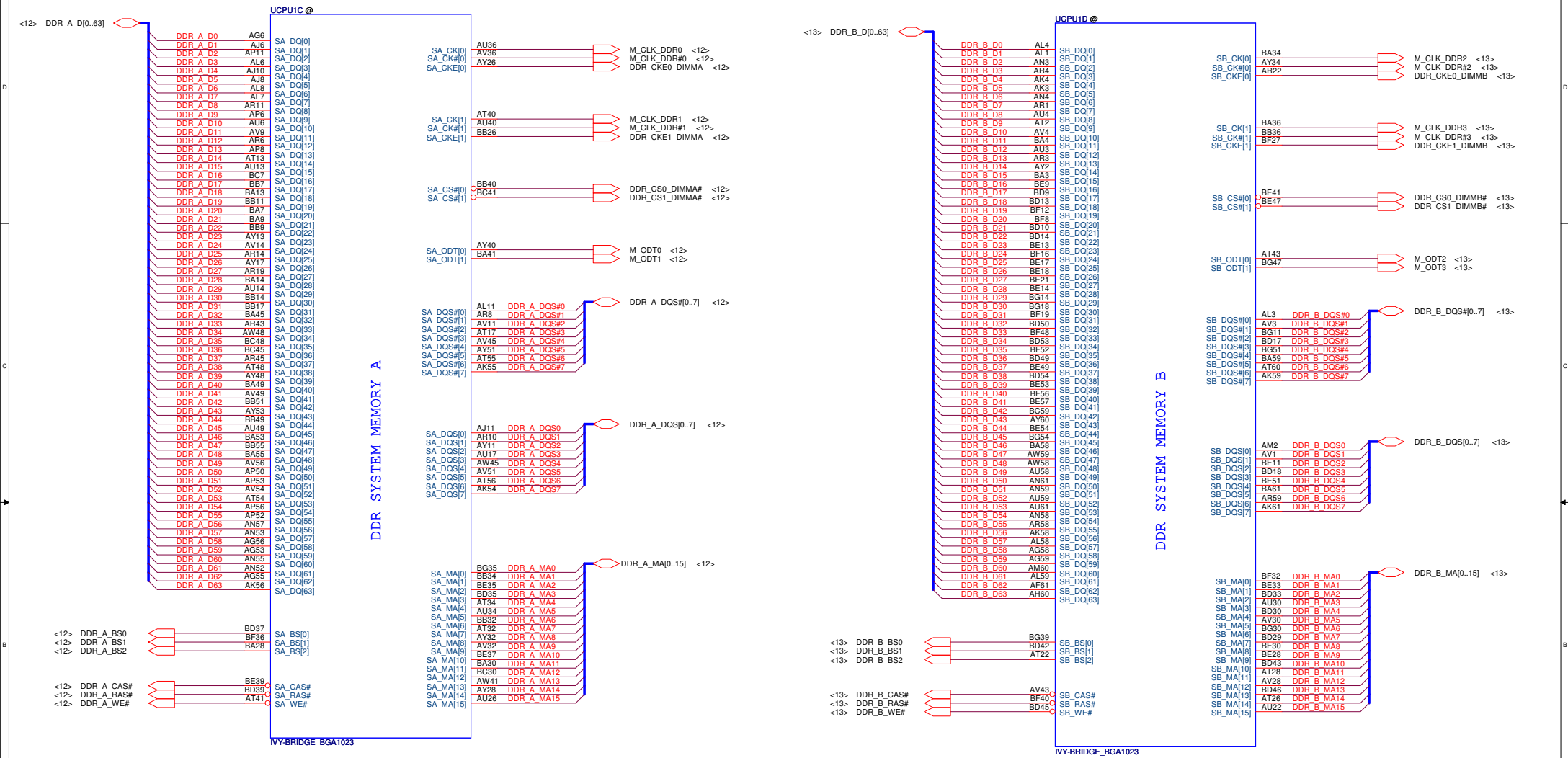
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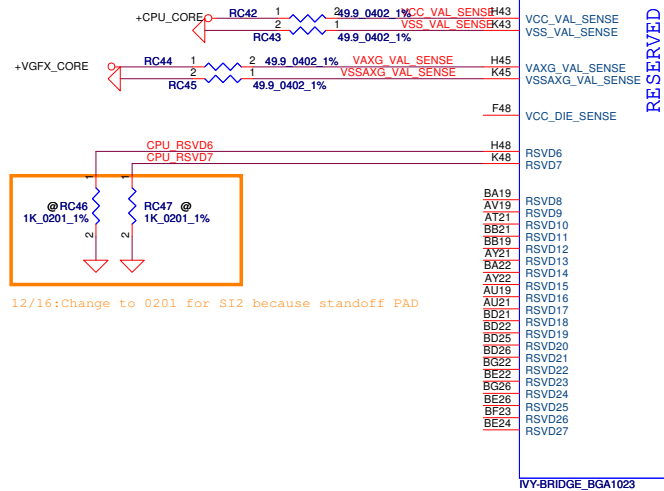


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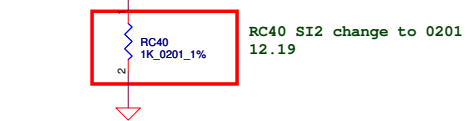
Change to part G.

Delete T12, T13, T10
12.212011.10.18 delete XDP resistor
just reserve test point for XDP.

CFG Straps for Processor

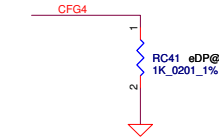
PEG bus is reversed, need to PD.

11.01



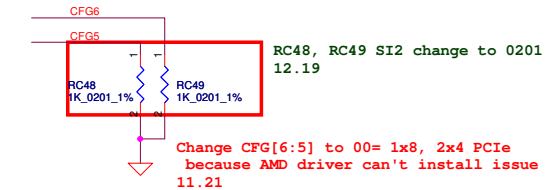
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	<p>★ 1: Normal Operation; Lane # definition matches socket pin map definition</p> <p>0: Lane Reversed</p>
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Display Port Presence Strap

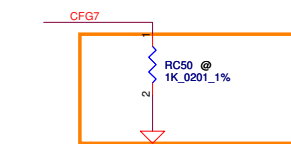
CFG4	<p>★ 1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>
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PCIe Port Bifurcation Straps

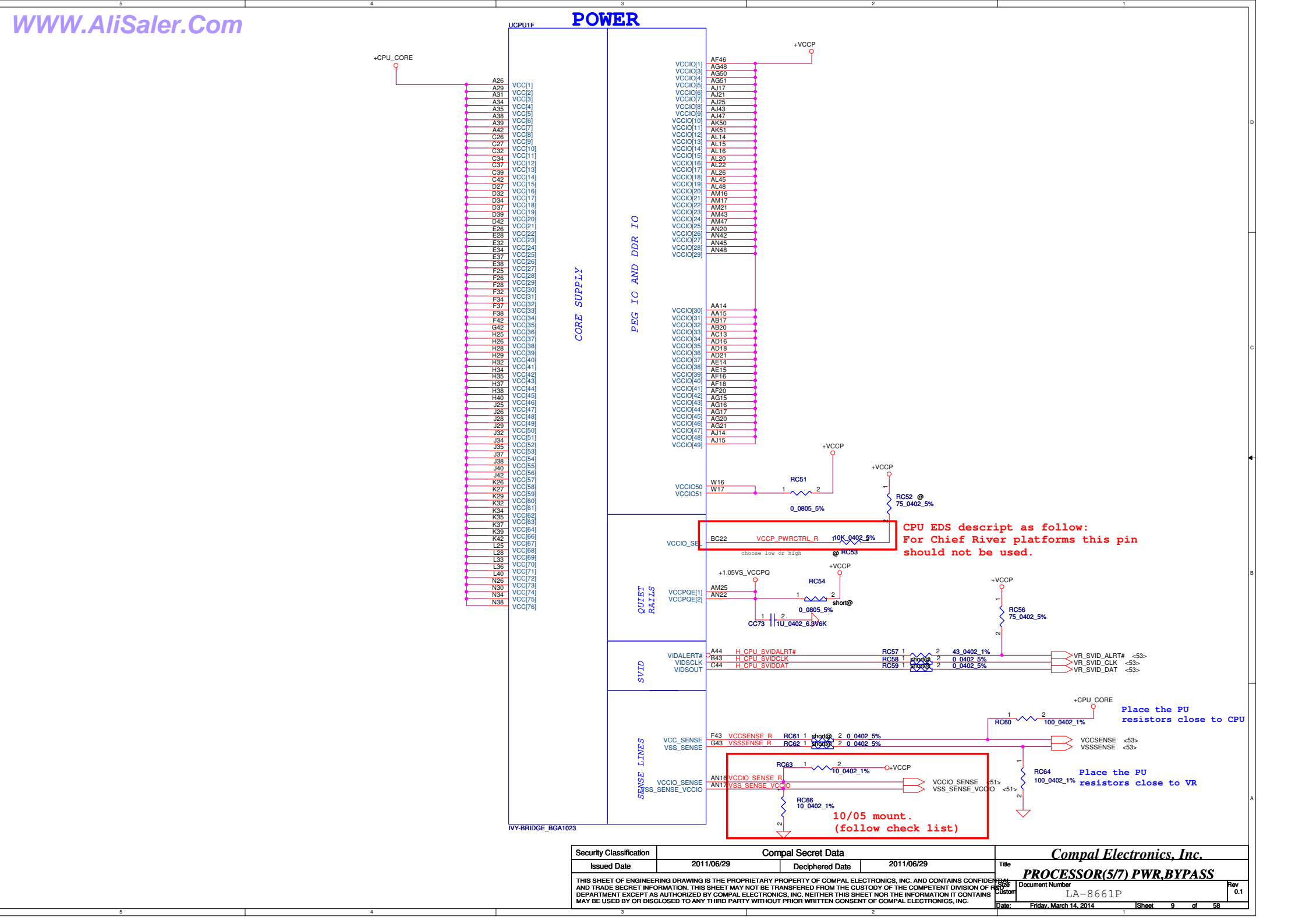
CFG[6:5]	<p>★ 00 = 1 x 8, 2 x 4 PCI Express</p> <p>01 = reserved</p> <p>10 = 2 x 8 PCI Express</p> <p>11 = 1 x 16 PCI Express</p>
----------	--

12/16: Change to 0201 for SI2 because standoff PAD



PEG DEFER TRAINING

CFG7	<p>★ 1: (Default) PEG Train immediately following xRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>
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The diagram illustrates the PCB layout for the Processor(5/7) PWR,BYPASS section, organized into several functional areas:

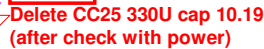
- CORE SUPPLY:** Features a large array of VCC pins (VCC[1] to VCC[76]) connected to a +CPU_CORE supply. A separate +VCCP supply is also shown.
- POWER:** Includes various VCCI pins (VCCI[1] to VCCI[49]) connected to +VCCP supplies.
- PEG IO AND DDR IO:** Contains VCCIO pins (VCCIO[30] to VCCIO[49]) connected to +VCCP supplies.
- QUIET RAILS:** Shows connections for VCCPQE[1], VCCPQE[2], and VCCPQE[3] to +VCCP supplies, along with resistors RC51, RC52, RC53, RC54, and RC55.
- SVID:** Displays VIDALERT#, VIDCLK, and VIDOUT signals connected to +VCCP supplies via resistors RC56, RC57, RC58, and RC59.
- SENSE LINES:** Includes VCC_SENSE, VSS_SENSE, VCCIO_SENSE, and VSS_SENSE_VCCIO signals connected to +VCCP supplies via resistors RC60, RC61, RC62, RC63, RC64, and RC65.

Annotations and Notes:

- CPU EDS descript as follow:** For Chief River platforms this pin should not be used.
- Place the PU resistors close to CPU**
- Place the PU resistors close to VR**
- 10/05 mount. (follow check list)**

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POWER

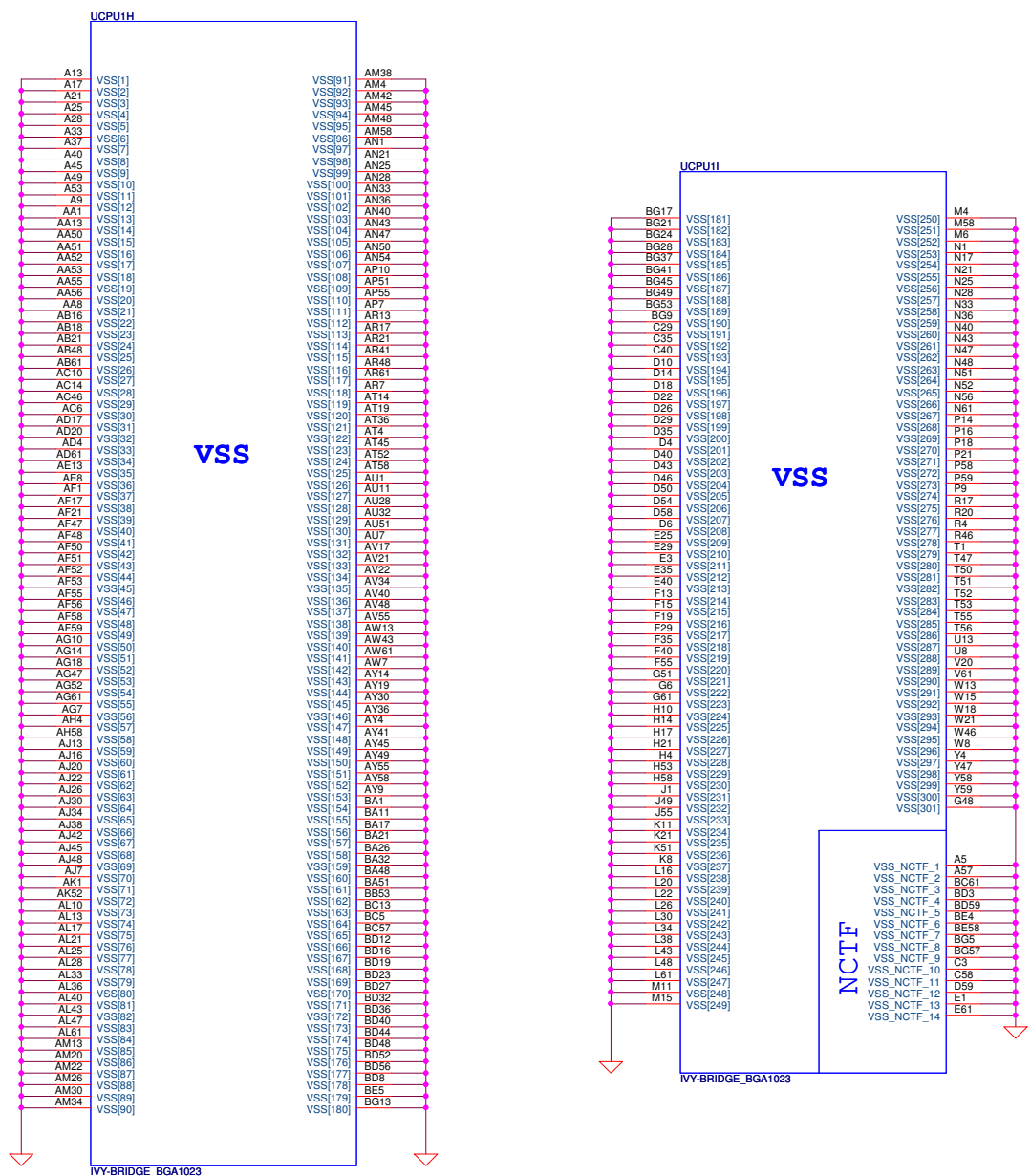


SENSE LINES



VID[0]	VID[1]		2011	2012
0	0	0.90 V	Yes	Yes
0	1	0.80 V	Yes	Yes
1	0	0.725 V	No	Yes
1	1	0.675 V	No	Yes

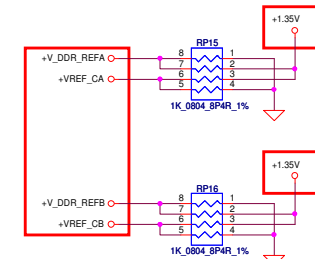
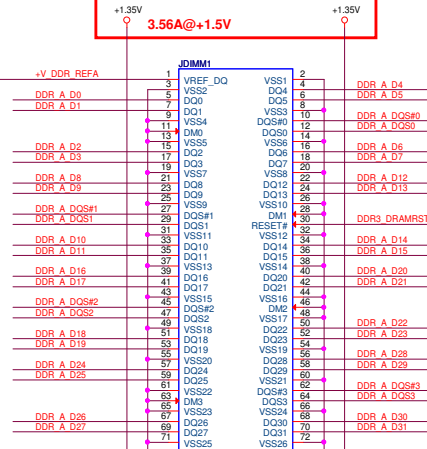
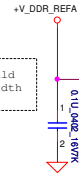
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DDR3 SO-DIMM A

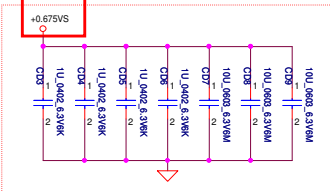
<7> DDR_A_D0[0..63]
<7> DDR_A_D0S[0..7]
<7> DDR_A_D0S#0[0..7]
<7> DDR_A_MA[0..15]

All VREF traces should have 20 mil trace width



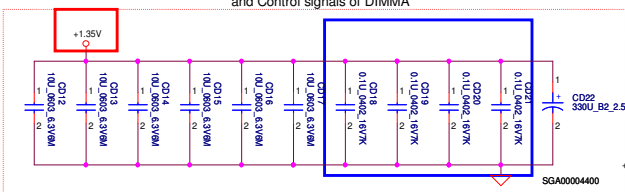
<1120>Swap assignment.

Layout Note:
Place near JDIMM1.203 & JDIMM1.204

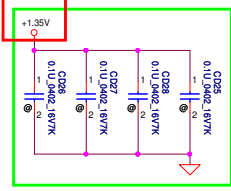


Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



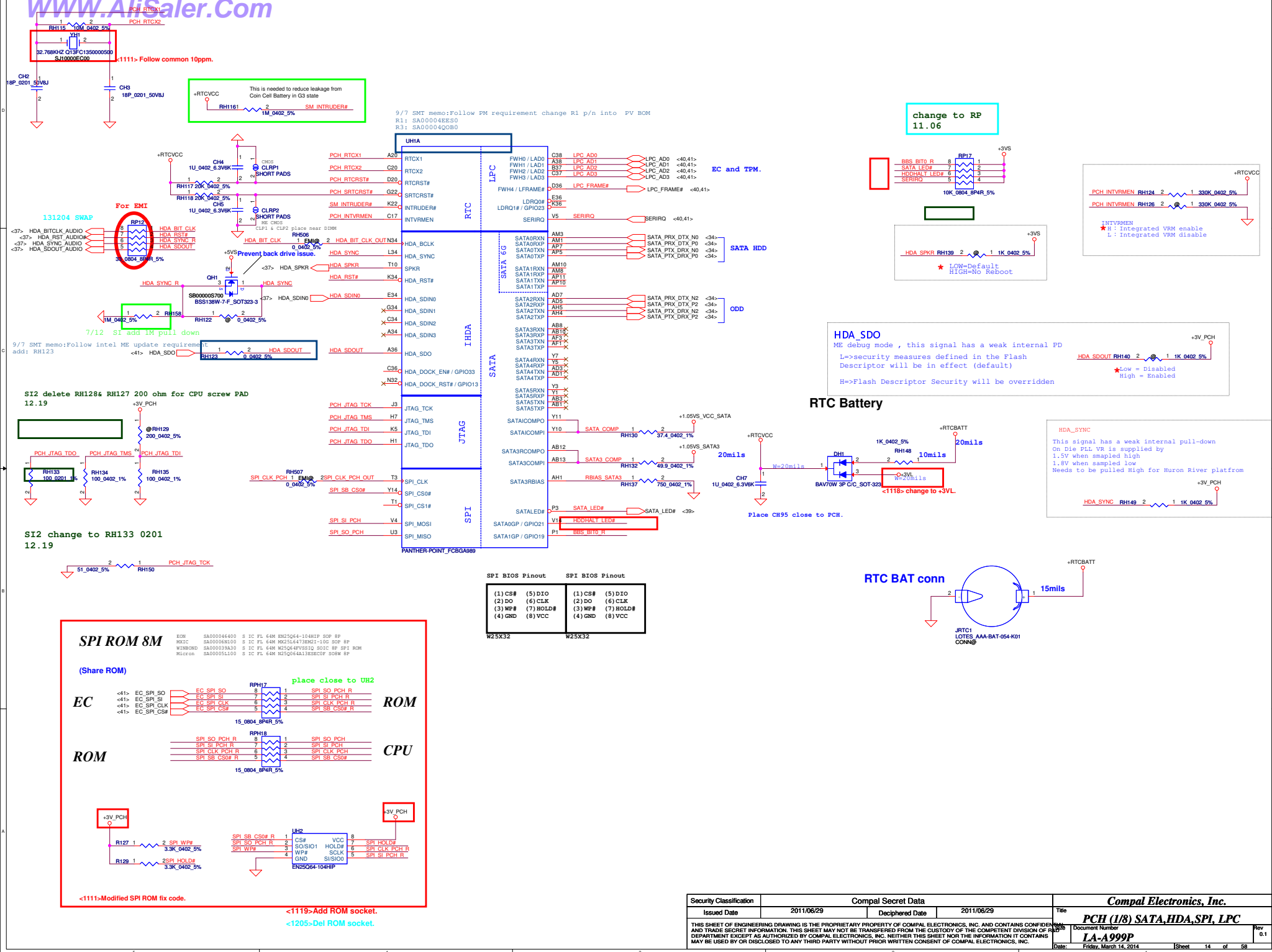
DDR3 SO-DIMM A

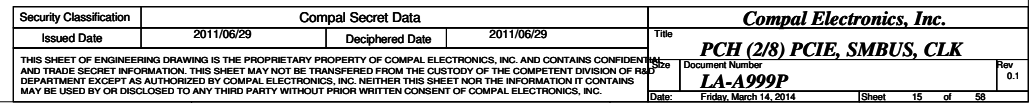


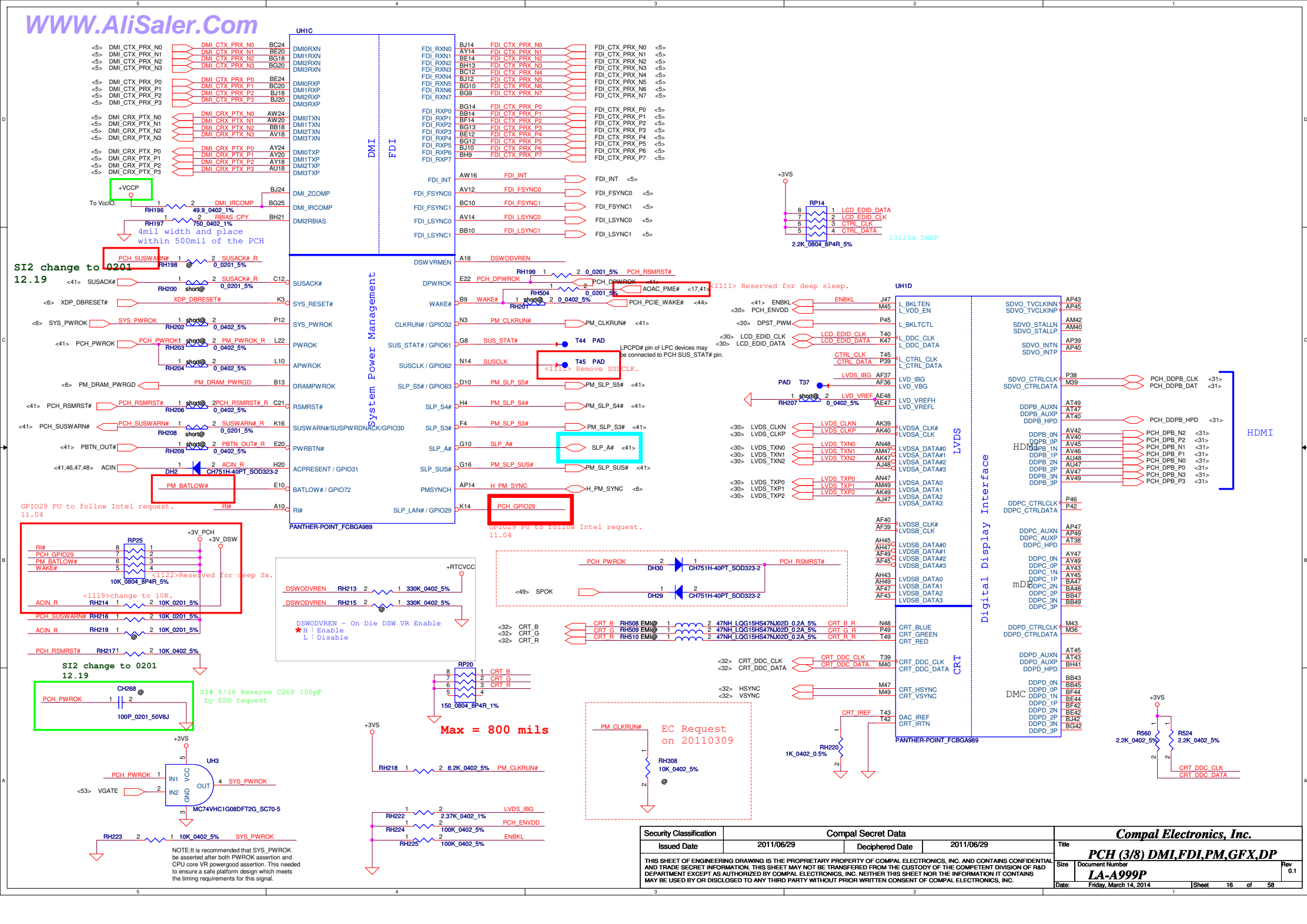
SI# 8/16 Reserve 4 pcs 0.1uF for EMI noise issue

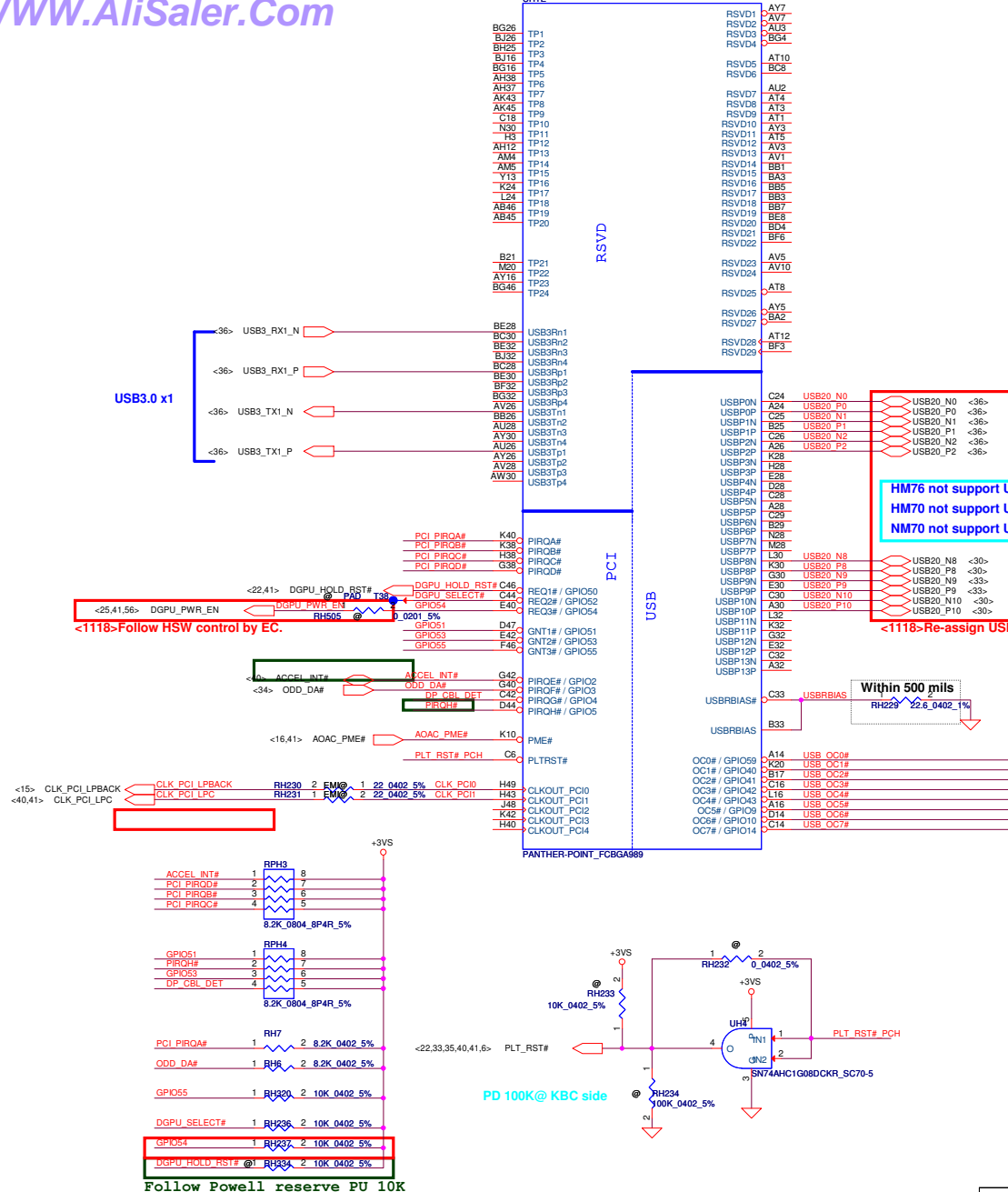
Standard
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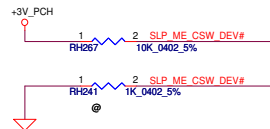




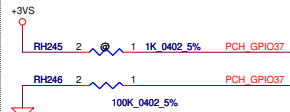
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GPIO28

On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

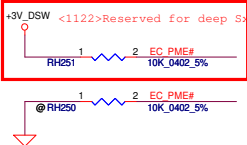


PCH_GPIO37
FDI TERMINATION VOLTAGE OVERRIDE
★ LOW - Tx, Rx terminated to same voltage (DC Coupling Mode)

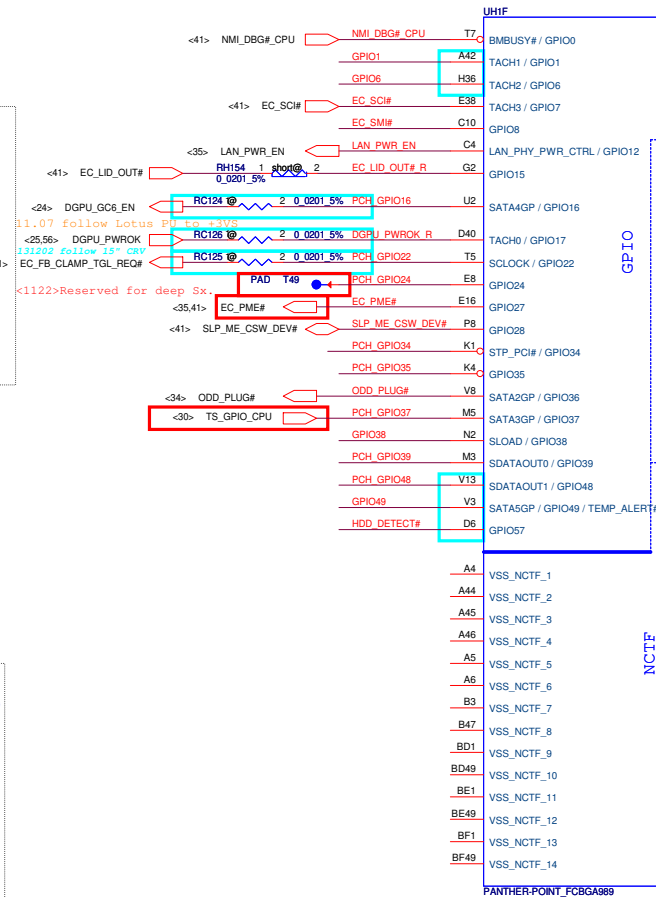


GPIO27

PCH_GPIO27 (Have internal Pull-High)
★ High: VCCVRM VR Enable
Low: VCCVRM VR Disable



DB# 10/20 Reserve GPIO 36 pull up resistor and add pull down resistor



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The diagram illustrates the power distribution network for the PCH (6/8) PWR. It features several main power rails and their associated components:

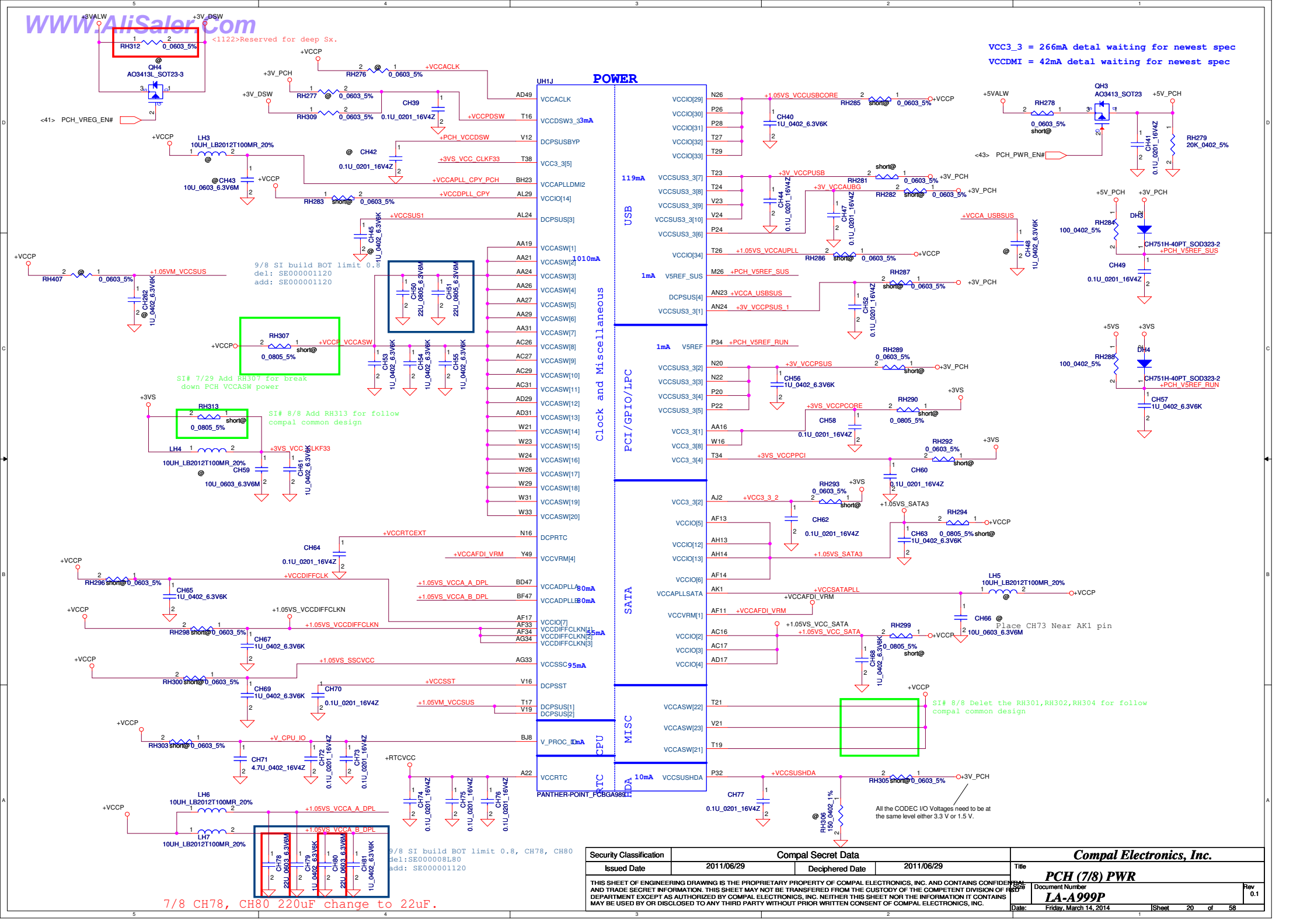
- VCC CORE:** Includes VCCOAC, VSSADAC, VCCALVDS, VSSALVDS, and VCCTX_LVDS[1-4].
- HVCMOS:** Includes VCC3_3[6], VCC3_3[7], VCCVRM[3], VCCDM[1], VCCCLKDMI, and VCC3_3[3].
- VCCIO:** Includes VCCIO[28], VCCIO[15], VCCIO[16], VCCIO[17], VCCIO[18], VCCIO[19], VCCIO[20], VCCIO[21], VCCIO[22], VCCIO[23], VCCIO[24], VCCIO[25], VCCIO[26], VCC3_3[3], VCCVRM[2], VCCAFDIPLL, VCCIO[27], and VCCDM[2].
- FDI:** Includes VCCDFTERM[1-4], VCCSPI, and VCCAFDI_VRM.

Key components and annotations include:

- Capacitors:** CH17, CH19, CH20, CH21, CH22, CH23, CH24, CH25, CH26, CH27, CH28, CH29, CH30, CH31, CH32, CH33, CH34, CH35, CH36, CH37, CH38, CH39, CH40, CH41, CH42, CH43, CH44, CH45, CH46, CH47, CH48, CH49, CH50, CH51, CH52, CH53, CH54, CH55, CH56, CH57, CH58, CH59, CH60, CH61, CH62, CH63, CH64, CH65, CH66, CH67, CH68, CH69, CH70, CH71, CH72, CH73, CH74, CH75, CH76, CH77, CH78, CH79, CH80, CH81, CH82, CH83, CH84, CH85, CH86, CH87, CH88, CH89, CH90, CH91, CH92, CH93, CH94, CH95, CH96, CH97, CH98, CH99, CH100.
- Resistors:** RH264, RH265, RH266, RH267, RH268, RH269, RH270, RH271, RH272, RH273, RH274, RH275, RH276, RH277, RH278, RH279, RH280, RH281, RH282, RH283, RH284, RH285, RH286, RH287, RH288, RH289, RH290, RH291, RH292, RH293, RH294, RH295, RH296, RH297, RH298, RH299, RH300.
- Inductors:** LH1, LH2, LH3, LH4, LH5, LH6, LH7, LH8, LH9, LH10, LH11, LH12, LH13, LH14, LH15, LH16, LH17, LH18, LH19, LH20, LH21, LH22, LH23, LH24, LH25, LH26, LH27, LH28, LH29, LH30, LH31, LH32, LH33, LH34, LH35, LH36, LH37, LH38, LH39, LH40, LH41, LH42, LH43, LH44, LH45, LH46, LH47, LH48, LH49, LH50, LH51, LH52, LH53, LH54, LH55, LH56, LH57, LH58, LH59, LH60, LH61, LH62, LH63, LH64, LH65, LH66, LH67, LH68, LH69, LH70, LH71, LH72, LH73, LH74, LH75, LH76, LH77, LH78, LH79, LH80, LH81, LH82, LH83, LH84, LH85, LH86, LH87, LH88, LH89, LH90, LH91, LH92, LH93, LH94, LH95, LH96, LH97, LH98, LH99, LH100.
- Annotations:** "2011.10.18 change all cap to small size: 22uF 10uF to 0603, 4.7uF to 0402, 1uF, 0.1uF, 0.01uF to 0201", "SI# 8/8 Add RH297 for power break down", "SI# 8/8 Change 10uH to 0805 0 ohm to follow compal common design", "Change BIOS ROM power rail to +3V_PCH 2014.01.21", "Place CH35 Near AP13, AP15 pin", "Place CH37 Near AP19 pin", "Place CH38 Near AP13, AP15 pin", "Place CH39 Near AP13, AP15 pin", "Place CH40 Near AP13, AP15 pin", "Place CH41 Near AP13, AP15 pin", "Place CH42 Near AP13, AP15 pin", "Place CH43 Near AP13, AP15 pin", "Place CH44 Near AP13, AP15 pin", "Place CH45 Near AP13, AP15 pin", "Place CH46 Near AP13, AP15 pin", "Place CH47 Near AP13, AP15 pin", "Place CH48 Near AP13, AP15 pin", "Place CH49 Near AP13, AP15 pin", "Place CH50 Near AP13, AP15 pin", "Place CH51 Near AP13, AP15 pin", "Place CH52 Near AP13, AP15 pin", "Place CH53 Near AP13, AP15 pin", "Place CH54 Near AP13, AP15 pin", "Place CH55 Near AP13, AP15 pin", "Place CH56 Near AP13, AP15 pin", "Place CH57 Near AP13, AP15 pin", "Place CH58 Near AP13, AP15 pin", "Place CH59 Near AP13, AP15 pin", "Place CH60 Near AP13, AP15 pin", "Place CH61 Near AP13, AP15 pin", "Place CH62 Near AP13, AP15 pin", "Place CH63 Near AP13, AP15 pin", "Place CH64 Near AP13, AP15 pin", "Place CH65 Near AP13, AP15 pin", "Place CH66 Near AP13, AP15 pin", "Place CH67 Near AP13, AP15 pin", "Place CH68 Near AP13, AP15 pin", "Place CH69 Near AP13, AP15 pin", "Place CH70 Near AP13, AP15 pin", "Place CH71 Near AP13, AP15 pin", "Place CH72 Near AP13, AP15 pin", "Place CH73 Near AP13, AP15 pin", "Place CH74 Near AP13, AP15 pin", "Place CH75 Near AP13, AP15 pin", "Place CH76 Near AP13, AP15 pin", "Place CH77 Near AP13, AP15 pin", "Place CH78 Near AP13, AP15 pin", "Place CH79 Near AP13, AP15 pin", "Place CH80 Near AP13, AP15 pin", "Place CH81 Near AP13, AP15 pin", "Place CH82 Near AP13, AP15 pin", "Place CH83 Near AP13, AP15 pin", "Place CH84 Near AP13, AP15 pin", "Place CH85 Near AP13, AP15 pin", "Place CH86 Near AP13, AP15 pin", "Place CH87 Near AP13, AP15 pin", "Place CH88 Near AP13, AP15 pin", "Place CH89 Near AP13, AP15 pin", "Place CH90 Near AP13, AP15 pin", "Place CH91 Near AP13, AP15 pin", "Place CH92 Near AP13, AP15 pin", "Place CH93 Near AP13, AP15 pin", "Place CH94 Near AP13, AP15 pin", "Place CH95 Near AP13, AP15 pin", "Place CH96 Near AP13, AP15 pin", "Place CH97 Near AP13, AP15 pin", "Place CH98 Near AP13, AP15 pin", "Place CH99 Near AP13, AP15 pin", "Place CH100 Near AP13, AP15 pin".

PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLL	1.05	0.08
VccADPLL	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

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H5		UH1H	
	VSS[0]		
AA17	VSS[1]	VSS[80]	AK38
AA2	VSS[2]	VSS[81]	AK4
AA3	VSS[3]	VSS[82]	AK42
AA33	VSS[4]	VSS[83]	AK46
AA34	VSS[5]	VSS[84]	AK8
AB11	VSS[6]	VSS[85]	AL16
AB14	VSS[7]	VSS[86]	AL17
AB39	VSS[8]	VSS[87]	AL19
AB4	VSS[9]	VSS[88]	AL2
AB43	VSS[10]	VSS[89]	AL21
AB5	VSS[11]	VSS[90]	AL23
AB7	VSS[12]	VSS[91]	AL26
AC19	VSS[13]	VSS[92]	AL27
AC2	VSS[14]	VSS[93]	AL31
AC21	VSS[15]	VSS[94]	AL33
AC24	VSS[16]	VSS[95]	AL34
AC33	VSS[17]	VSS[96]	AL48
AC34	VSS[18]	VSS[97]	AM11
AC48	VSS[19]	VSS[98]	AM14
AD10	VSS[20]	VSS[99]	AM36
AD11	VSS[21]	VSS[100]	AM39
AD12	VSS[22]	VSS[101]	AM43
AD13	VSS[23]	VSS[102]	AM45
AD19	VSS[24]	VSS[103]	AM46
AD24	VSS[25]	VSS[104]	AM7
AD26	VSS[26]	VSS[105]	AN2
AD27	VSS[27]	VSS[106]	AN29
AD33	VSS[28]	VSS[107]	AN3
AD34	VSS[29]	VSS[108]	AN11
AD36	VSS[30]	VSS[109]	AP12
AD37	VSS[31]	VSS[110]	AP19
AD38	VSS[32]	VSS[111]	AP28
AD39	VSS[33]	VSS[112]	AP30
AD4	VSS[34]	VSS[113]	AP32
AD40	VSS[35]	VSS[114]	AP38
AD42	VSS[36]	VSS[115]	AP4
AD43	VSS[37]	VSS[116]	AP42
AD45	VSS[38]	VSS[117]	AP46
AD46	VSS[39]	VSS[118]	AP8
AD8	VSS[40]	VSS[119]	AR2
AE2	VSS[41]	VSS[120]	AR46
AE3	VSS[42]	VSS[121]	AT11
AF10	VSS[43]	VSS[122]	AT13
AF12	VSS[44]	VSS[123]	AT18
AD14	VSS[45]	VSS[124]	AT22
AD16	VSS[46]	VSS[125]	AT26
AF16	VSS[47]	VSS[126]	AT28
AF19	VSS[48]	VSS[127]	AT30
AF24	VSS[49]	VSS[128]	AT32
AF26	VSS[50]	VSS[129]	AT34
AF27	VSS[51]	VSS[130]	AT39
AF29	VSS[52]	VSS[131]	AT42
AF31	VSS[53]	VSS[132]	AT46
AF36	VSS[54]	VSS[133]	AT7
AF4	VSS[55]	VSS[134]	AU24
AF42	VSS[56]	VSS[135]	AU30
AF46	VSS[57]	VSS[136]	AV16
AF5	VSS[58]	VSS[137]	AV20
AF7	VSS[59]	VSS[138]	AV24
AF8	VSS[60]	VSS[139]	AV30
AG19	VSS[61]	VSS[140]	AV38
AG2	VSS[62]	VSS[141]	AV4
AG31	VSS[63]	VSS[142]	AV43
AG48	VSS[64]	VSS[143]	AV8
AH11	VSS[65]	VSS[144]	AW14
AH3	VSS[66]	VSS[145]	AW18
AH36	VSS[67]	VSS[146]	AW2
AH39	VSS[68]	VSS[147]	AW26
AH40	VSS[69]	VSS[148]	AW28
AH42	VSS[70]	VSS[149]	AW32
AH46	VSS[71]	VSS[150]	AW34
AH7	VSS[72]	VSS[151]	AW36
AJ19	VSS[73]	VSS[152]	AW40
AJ21	VSS[74]	VSS[153]	AW48
AJ24	VSS[75]	VSS[154]	AV11
AJ33	VSS[76]	VSS[155]	AY12
AJ34	VSS[77]	VSS[156]	AY22
AK12	VSS[78]	VSS[157]	AY28
AK3	VSS[79]	VSS[158]	

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UH11		H46	
AY4	VSS[159]	VSS[259]	K18
AY42	VSS[160]	VSS[260]	K26
AY46	VSS[161]	VSS[261]	K39
AY8	VSS[162]	VSS[262]	K46
B11	VSS[163]	VSS[263]	K7
B15	VSS[164]	VSS[264]	L18
B19	VSS[165]	VSS[265]	L2
B23	VSS[166]	VSS[266]	L20
B27	VSS[167]	VSS[267]	L26
B31	VSS[168]	VSS[268]	L28
B35	VSS[169]	VSS[269]	L36
B39	VSS[170]	VSS[270]	L48
B7	VSS[171]	VSS[271]	M12
F45	VSS[172]	VSS[272]	P16
BB12	VSS[173]	VSS[273]	M18
BB16	VSS[174]	VSS[274]	M22
BB20	VSS[175]	VSS[275]	M24
BB22	VSS[176]	VSS[276]	M30
BB24	VSS[177]	VSS[277]	M32
BB28	VSS[178]	VSS[278]	M34
BB30	VSS[179]	VSS[279]	M38
BB38	VSS[180]	VSS[280]	M4
BB4	VSS[181]	VSS[281]	M42
BB46	VSS[182]	VSS[282]	M46
BC14	VSS[183]	VSS[283]	M6
BC18	VSS[184]	VSS[284]	N18
BC2	VSS[185]	VSS[285]	P30
BC22	VSS[186]	VSS[286]	N47
BC26	VSS[187]	VSS[287]	P11
BC32	VSS[188]	VSS[288]	P18
BC34	VSS[189]	VSS[289]	T33
BC36	VSS[190]	VSS[290]	P40
BC42	VSS[191]	VSS[291]	P43
BC46	VSS[192]	VSS[292]	P47
BD46	VSS[193]	VSS[293]	P7
BD5	VSS[194]	VSS[294]	R2
BE22	VSS[195]	VSS[295]	R48
BE26	VSS[196]	VSS[296]	T12
BE38	VSS[197]	VSS[297]	T31
BE40	VSS[198]	VSS[298]	T37
BF10	VSS[199]	VSS[299]	T4
BF12	VSS[200]	VSS[300]	W34
BF16	VSS[201]	VSS[301]	T46
BF20	VSS[202]	VSS[302]	T47
BF22	VSS[203]	VSS[303]	T8
BF24	VSS[204]	VSS[304]	V11
BF26	VSS[205]	VSS[305]	V17
BD3	VSS[206]	VSS[306]	V26
BF30	VSS[207]	VSS[307]	V27
BF36	VSS[208]	VSS[308]	V29
BF40	VSS[209]	VSS[309]	V31
BF8	VSS[210]	VSS[310]	V36
BG17	VSS[211]	VSS[311]	V39
BG21	VSS[212]	VSS[312]	V43
BG23	VSS[213]	VSS[313]	V7
BG44	VSS[214]	VSS[314]	W17
BG8	VSS[215]	VSS[315]	W19
BH11	VSS[216]	VSS[316]	W2
BH15	VSS[217]	VSS[317]	W27
BH17	VSS[218]	VSS[318]	W48
BH19	VSS[219]	VSS[319]	Y12
H10	VSS[220]	VSS[320]	Y38
BH27	VSS[221]	VSS[321]	Y4
BH31	VSS[222]	VSS[322]	Y42
BH33	VSS[223]	VSS[323]	Y46
BH35	VSS[224]	VSS[324]	Y8
BH39	VSS[225]	VSS[325]	BC29
BH43	VSS[226]	VSS[326]	N24
BH7	VSS[227]	VSS[327]	AJ3
D3	VSS[228]	VSS[328]	AD47
D12	VSS[229]	VSS[329]	B43
D16	VSS[230]	VSS[330]	BE10
D18	VSS[231]	VSS[331]	BG41
D22	VSS[232]	VSS[332]	G14
D24	VSS[233]	VSS[333]	H16
D26	VSS[234]	VSS[334]	T36
D30	VSS[235]	VSS[335]	BC22
D32	VSS[236]	VSS[336]	BG24
D34	VSS[237]	VSS[337]	C22
D38	VSS[238]	VSS[338]	AP13
D42	VSS[239]	VSS[339]	M14
D8	VSS[240]	VSS[340]	AP3
E18	VSS[241]	VSS[341]	AP7
E26	VSS[242]	VSS[342]	BE18
G18	VSS[243]	VSS[343]	BC16
G20	VSS[244]	VSS[344]	BG28
G26	VSS[245]	VSS[345]	BJ28
G28	VSS[246]	VSS[346]	
G36	VSS[247]		
G48	VSS[248]		
H12	VSS[249]		
H18	VSS[250]		
H22	VSS[251]		
H24	VSS[252]		
H26	VSS[253]		
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H32	VSS[255]		
H34	VSS[256]		
F3	VSS[257]		
	VSS[258]		

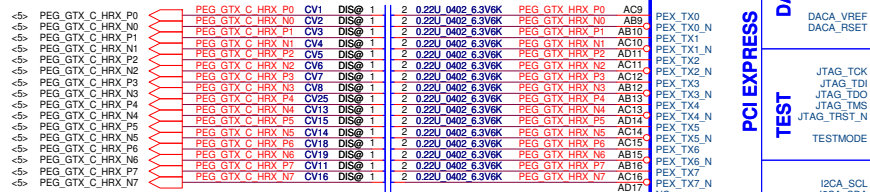
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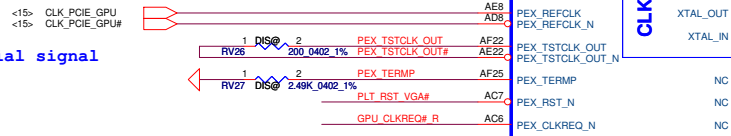


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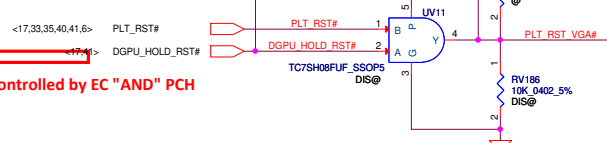
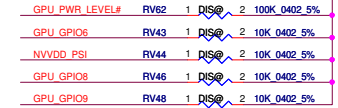


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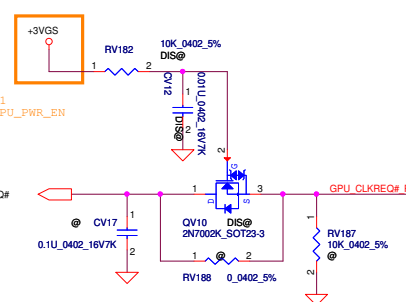
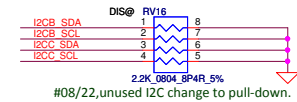
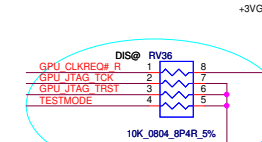
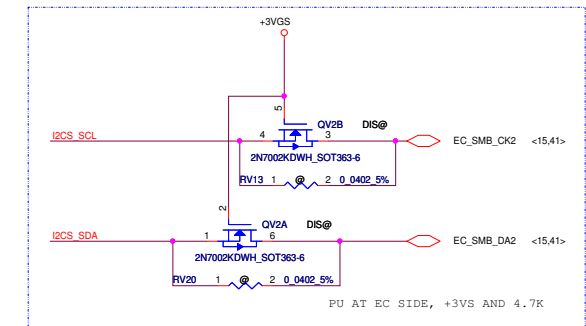
Differential signal



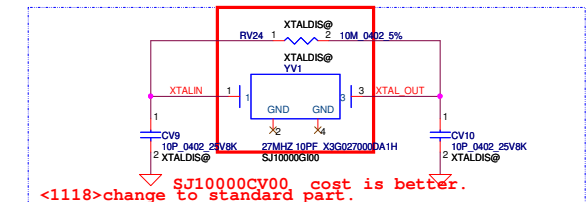
Controlled by EC "AND" PCH

#9/2 , Add RV191 between.
GPU_PWR_LEVEL# and GPU_THERMAL_DET##8/19 , N15V-GM didn't support GC6,
unpop QV13 , QV14.

131127 SWAP Pin of RV36.1, RV36.2 & RV36.4 by layout requested

SI 11/05 change RV182.1
change to +3VGS from GPU_PWR_EN

PU AT EC SIDE, +3VS AND 4.7K

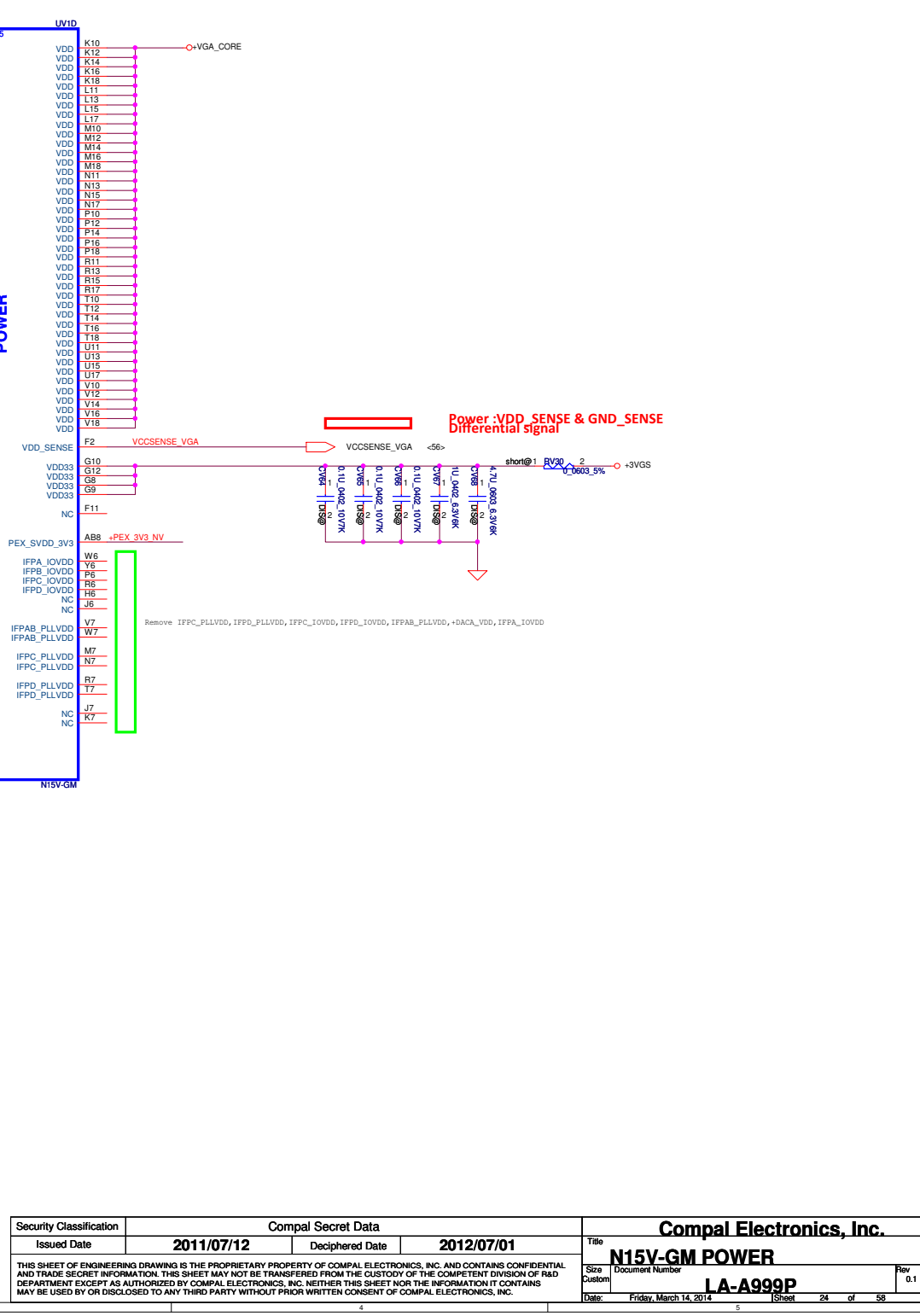
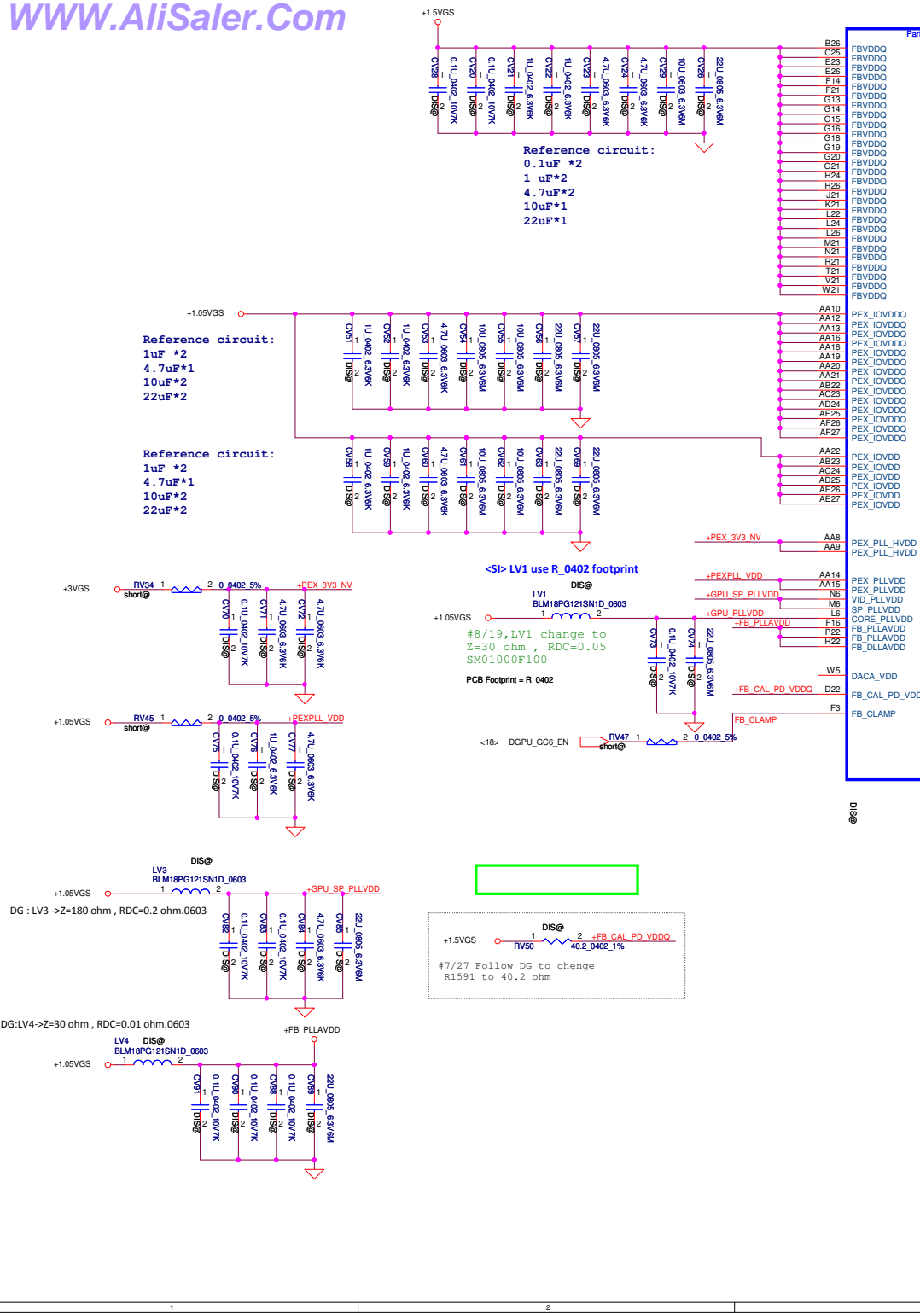


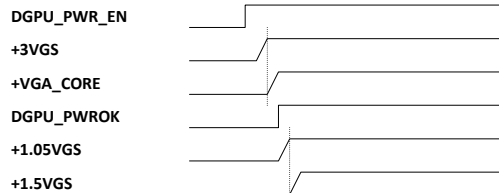
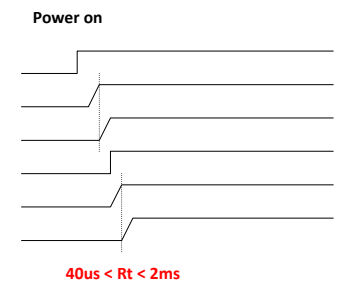
<1118>change to standard part.

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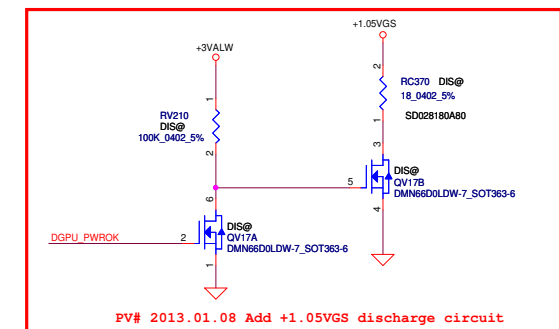
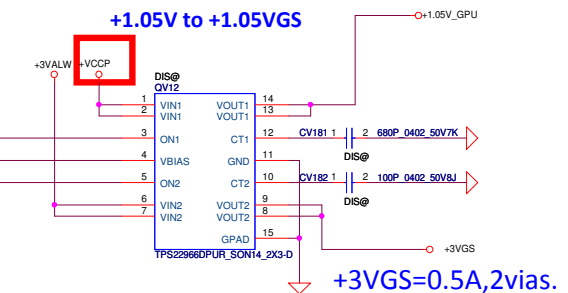
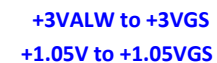


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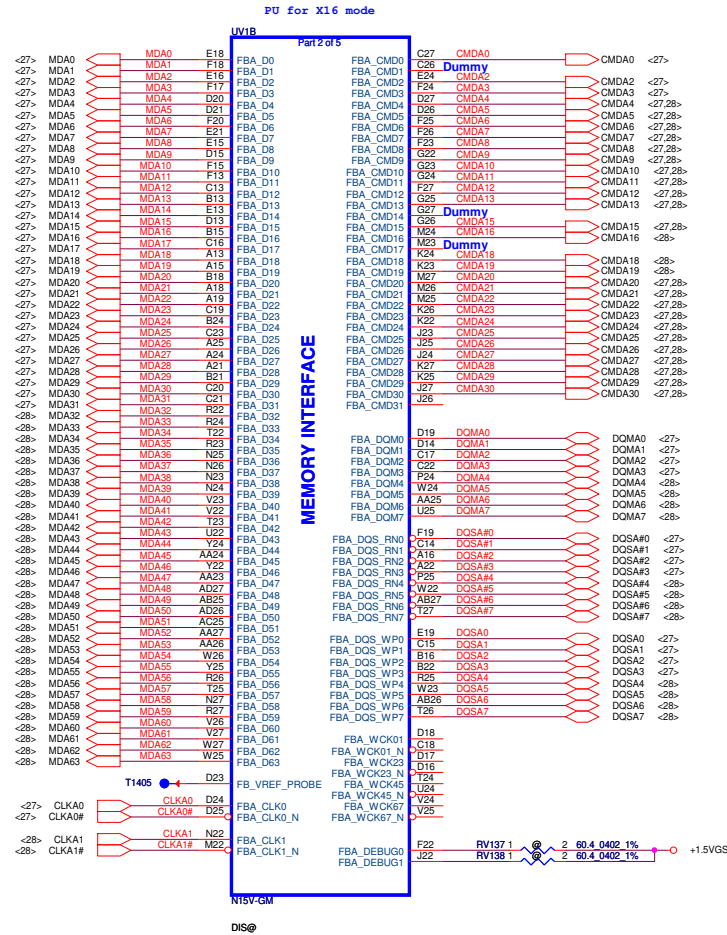




40us < Rt < 2ms



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Date:				Friday, March 14, 2014	Sheet	25 of 58

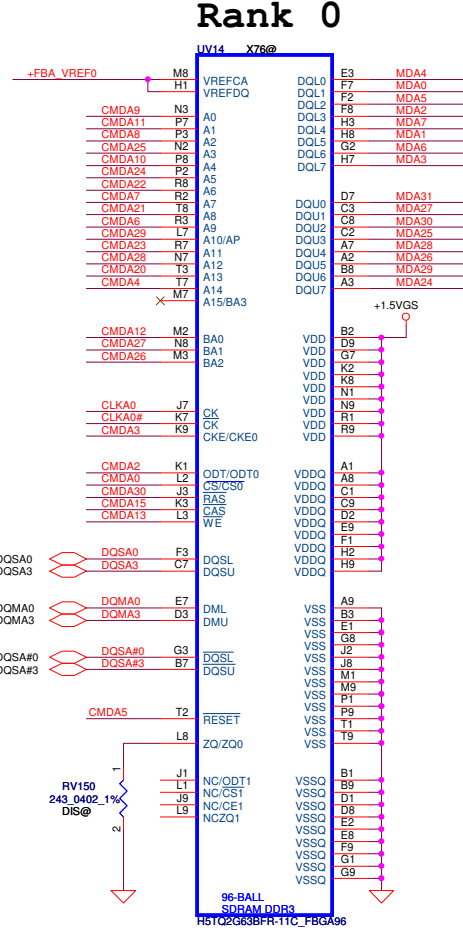
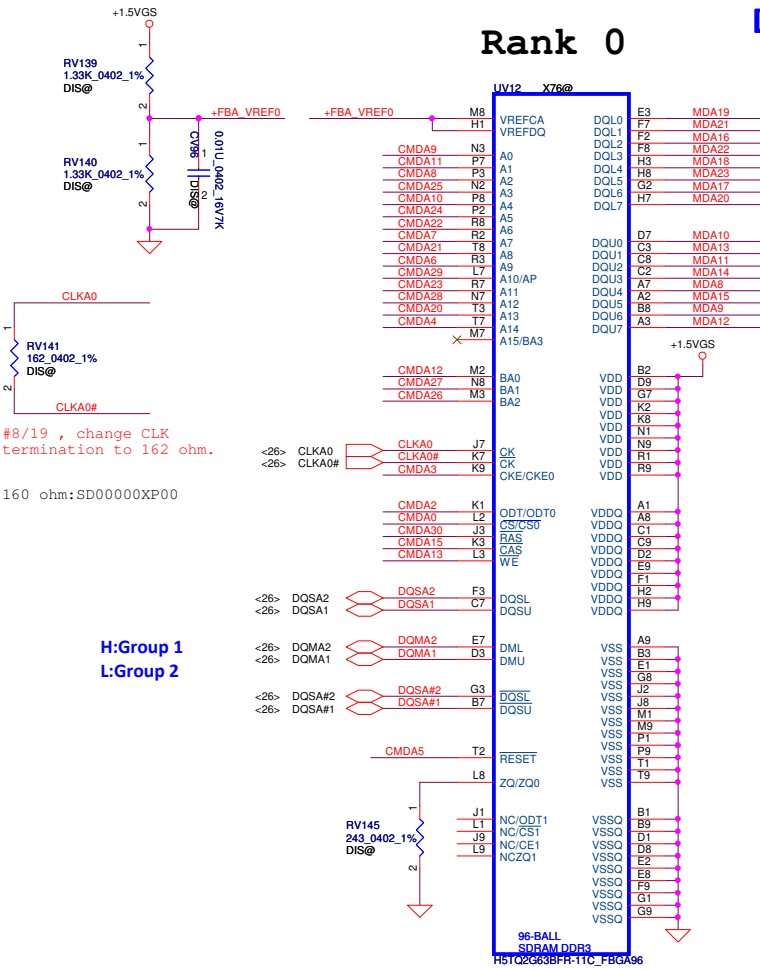


Mode D Command Mapping

RANK 0		
Address	0..31	32..63
FBx_CMD0	CS0#	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14		
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Data0~Data31

MDA[0..63] <26,28>
CMDA[30..0] <26,28>



Mode D Command Mapping

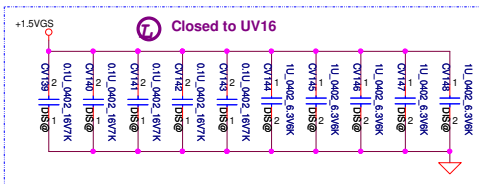
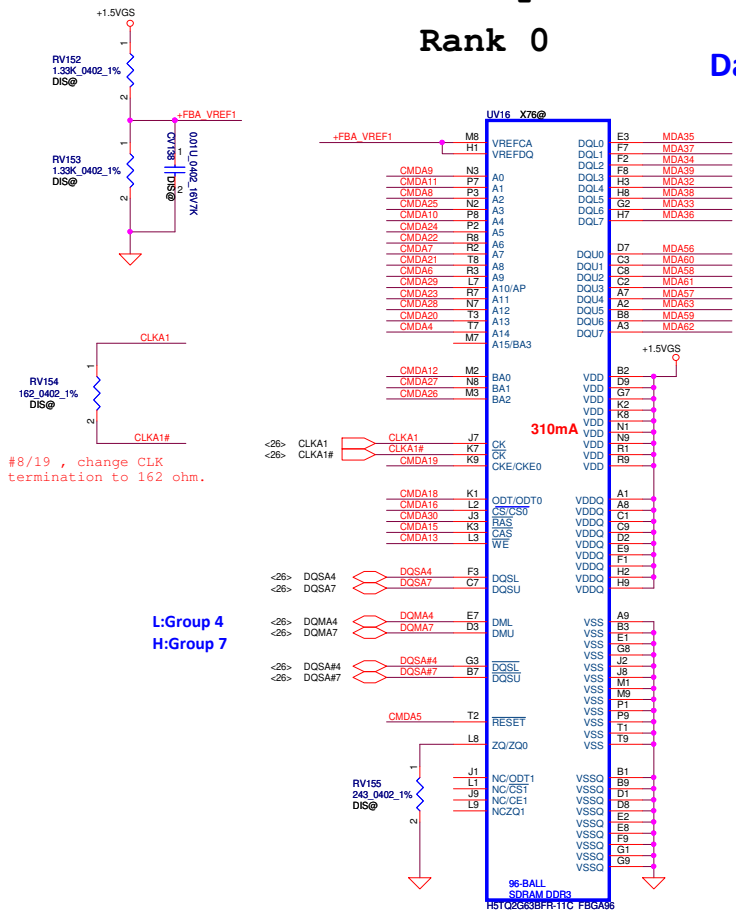
RANK 0		
Address	0..31	32..63
FBx_CMD0	CS0#	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14		
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Rank 0

Data32~Data63

Rank 0

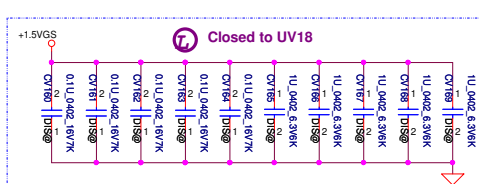
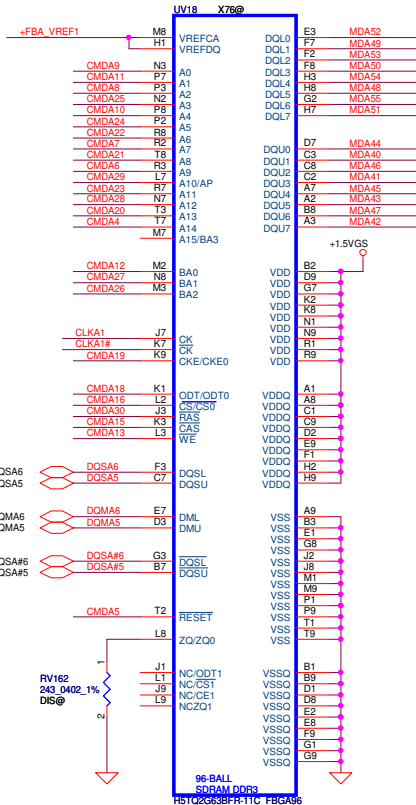
MDA[0..63] <26,27>
CMDA[30..0] <26,27>



Group 4

Group 7

L:Group 6
H:Group 5



Group 6

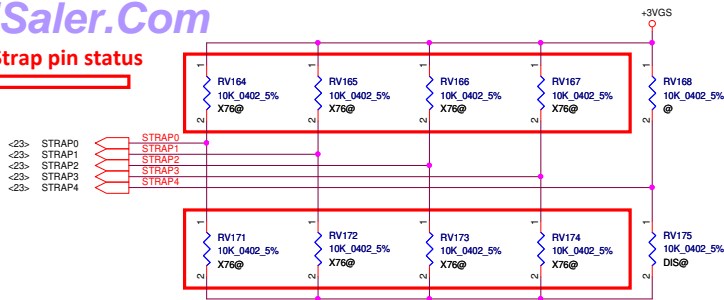
Group 5

Mode D Command Mapping

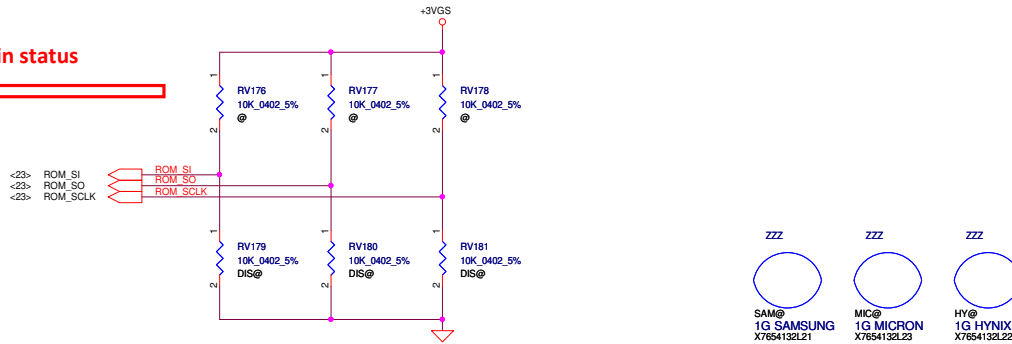
Address	0..31	32..63
FBx_CMD0	CS0#	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14		
FBx_CMD15	CAS#	CAS#
FBx_CMD16	CS0#	
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

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Compal Electronics, Inc.				N15V-GM VRAM C Lower	
Date: Friday, March 14, 2014				LA-A999P	
Sheet 28 of 58					

Check Strap pin status



Check SPI pin status



GPU	Project	VRAM size	CH	Description	Compal VRAM P/N	VRAM description	ROM CFG setup [3...0]	RAM_CFG	R P/N
N15V-GM (23x23) 64bit (One CH single rank)	ZSO40	128M(X16)	CHA	DDR3 Hynix 128Mx16 1.5V	SA00006H400	H5TC2G63FFR-11C 1000MHz	1100	RV171+RV172+RV167+RV166	
	ZSO50	128M(X16)	CHA	DDR3 Micron 128Mx16 1.5V	SA000067500	MT41J128M16JT-093G-K 1000MHz	0001	RV164+RV172+RV173+RV174	
		128M(X16)	CHA	DDR3 Samsung 128Mx16 1.5V	SA000068U00	K4W2G1646E-BC1A 1000MHz	0101	RV164+RV172+RV166+RV174	

#9/5 RAM_CFG follow RVL-06891-001 table 1.
Dule Rank layout with single Rank population.

Table 123

Strap pin Name	Strap Mapping	Resistance	Polarity	Logical Strapping Bit0
ROM_SCLK	SMB_ALT_ADDR	10K	Pull-down to GND.	
ROM_SI	SUB_VENDOR	10K	Pull-down to GND if no VBIOS ROM.	
ROM_SO	VGA_DEVICE	10K	Pull-down to GND(no diaplay).	
STRAP0	RAM_CFG[0]	10K		
STRAP1	RAM_CFG[1]	10K		
STRAP2	RAM_CFG[2]	10K		
STRAP3	RAM_CFG[3]	10K		
STRAP4	PCIE_MAX_SPEED	10K	Pull-down to GND(PCIE Gen1).	

SMBUS_ALT_ADDR

0	0x9E (Default)
1	0x9C (Multi-GPU usage)

SUB_VENDOR

0	Disable (Default)
1	

VGA_DEVICE

0	Non-Primary 3D Acceleration Device(Class Code 302h)(Default)
1	Primary Display or VGA Device .

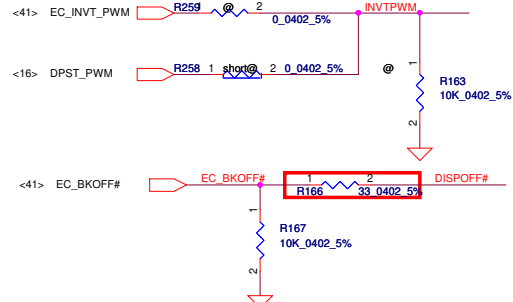
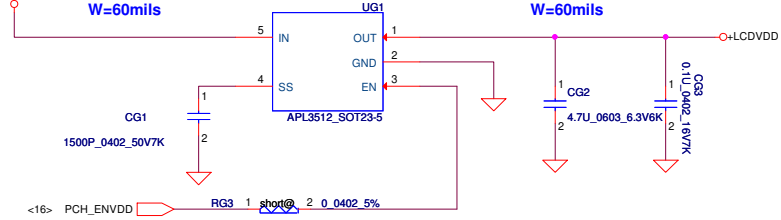
PCIE_MAX_SPEED

0	Limit to PCIe Gen1
1	PCIe Gen 2/3 Capable

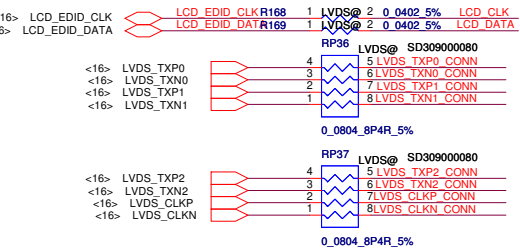
USER Straps

User [3:0]	
1000-1100	Customer defined

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	N15V-GM MISC	
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				Date: Friday, March 14, 2014	Sheet 29 of 58	LA-A999P

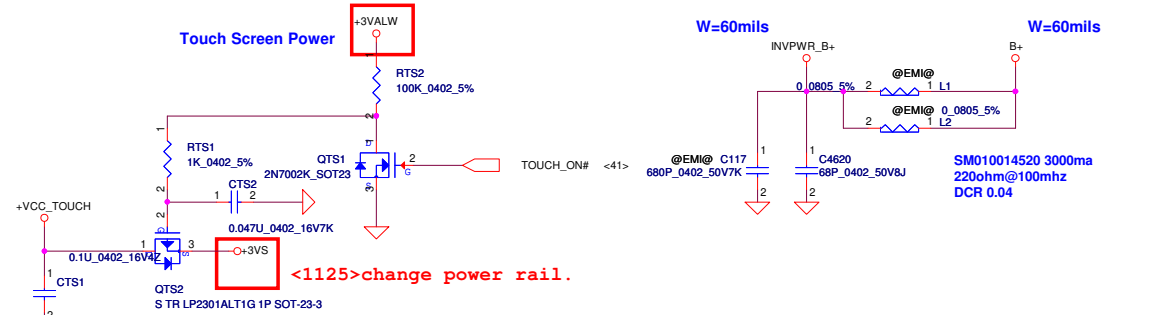
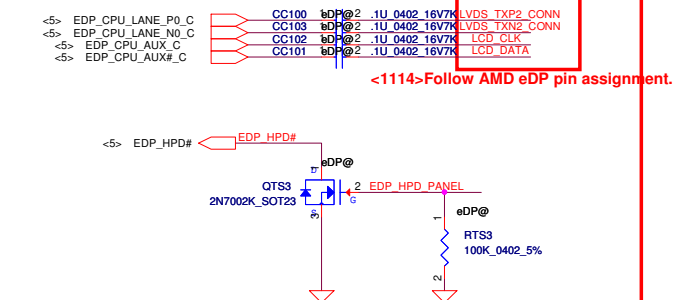


LVDS SKU

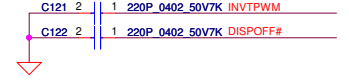
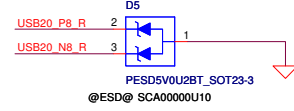
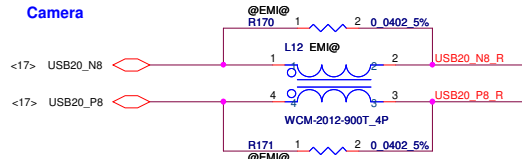


131203 SWAP

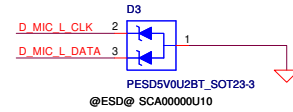
eDP SKU



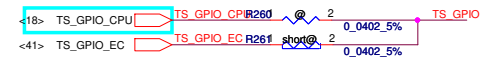
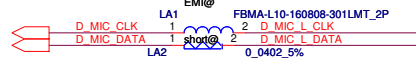
Camera



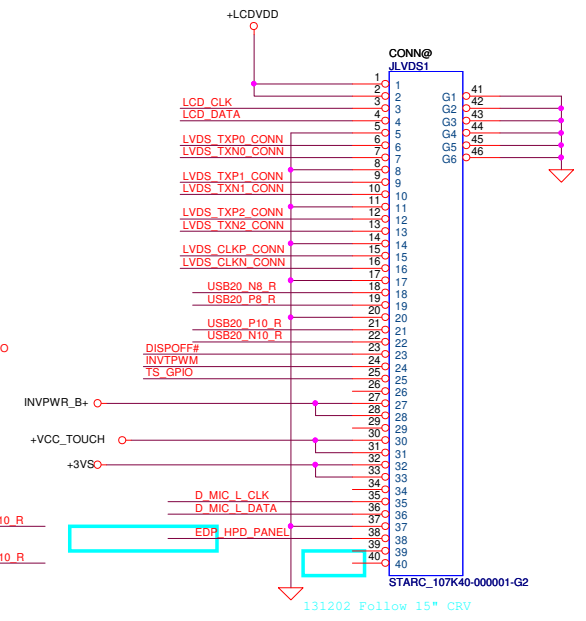
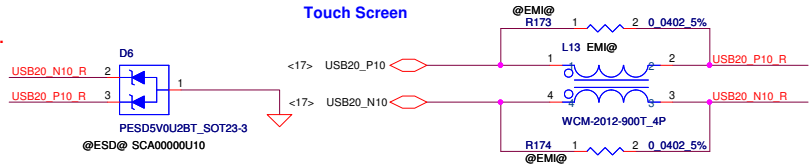
LCD/LED PANEL Conn.



<DB>LA1/LA2 closed to Aduio codec

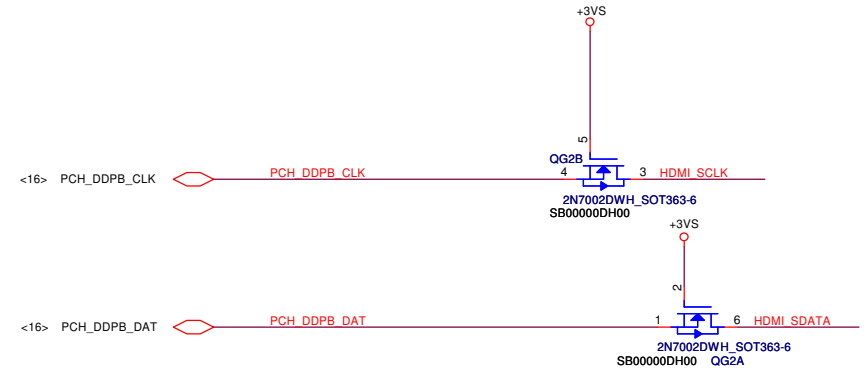
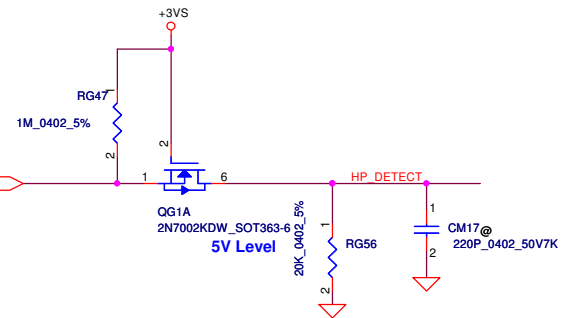
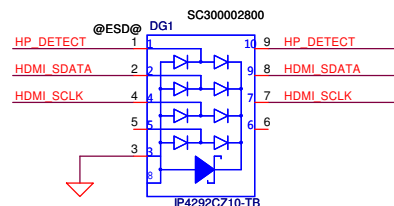
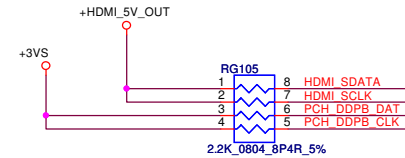
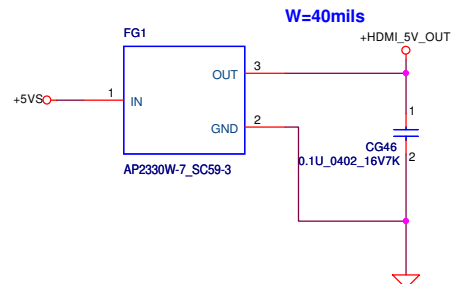
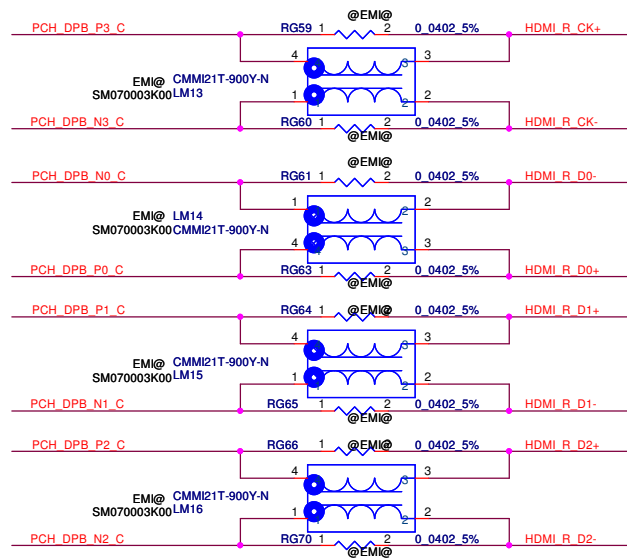
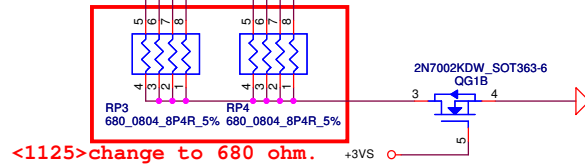
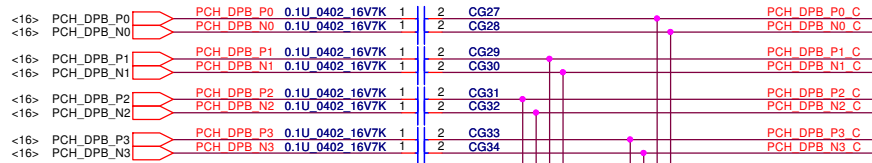


Touch Screen

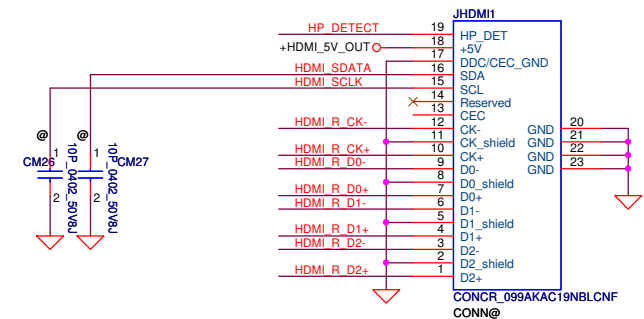


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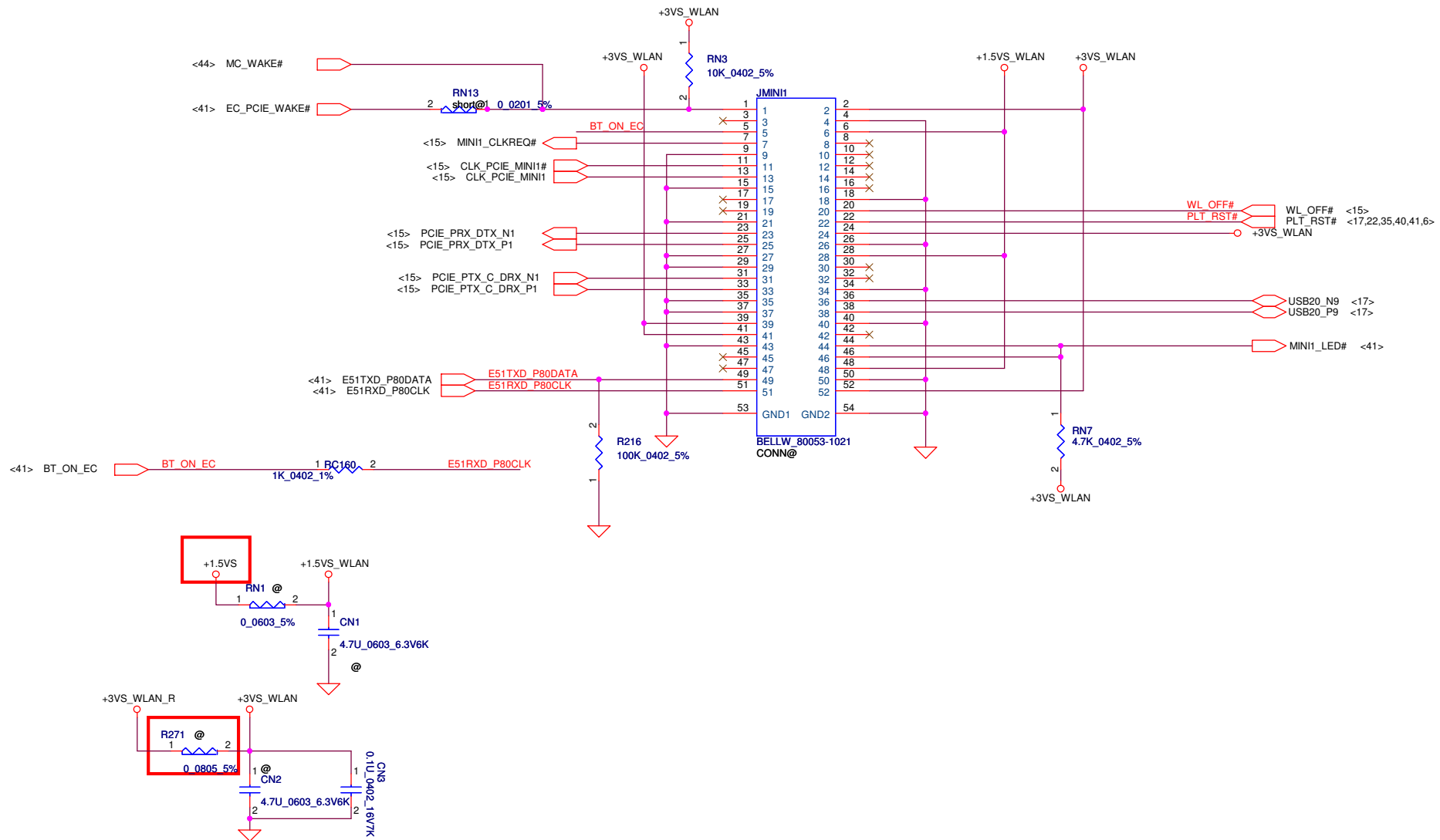
<CPU>



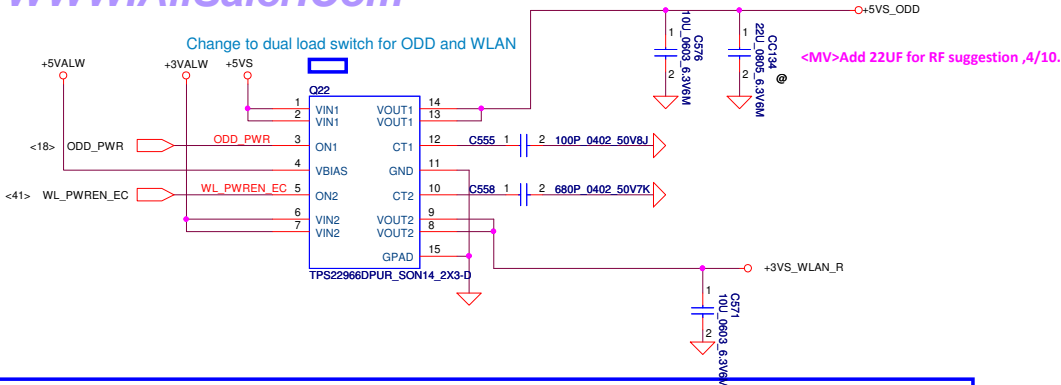
HDMI Conn.



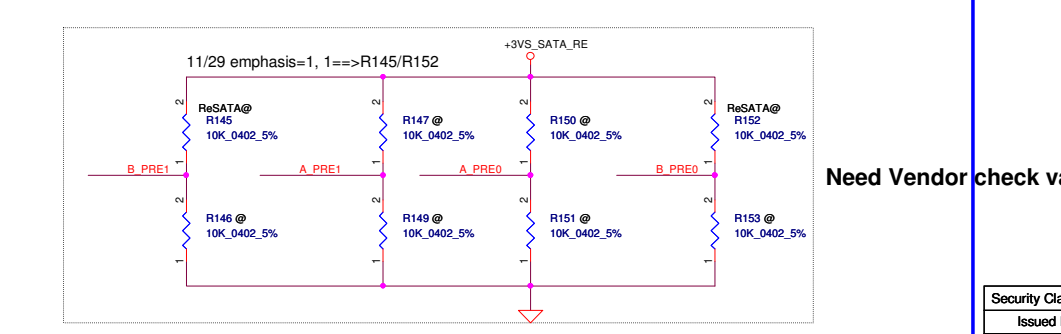
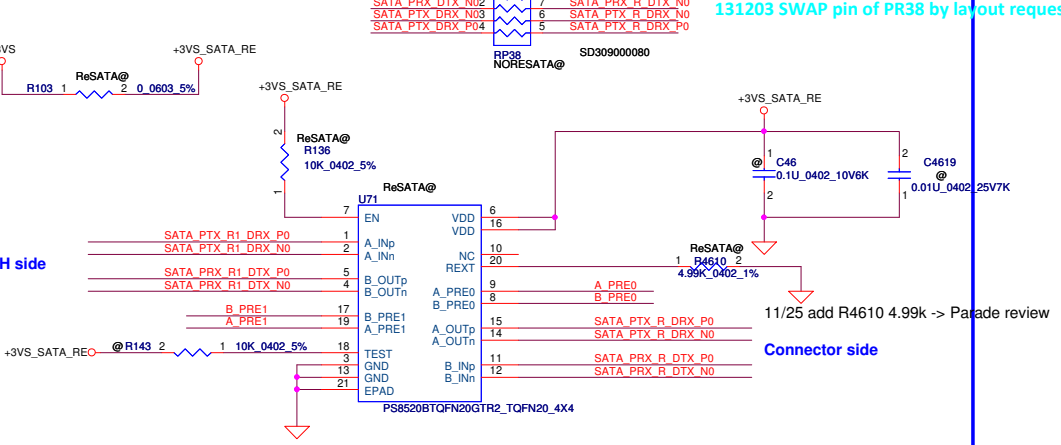
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Issued Date	2011/06/29	Deciphered Date	2011/06/29	HDMI Conn/Level shift	
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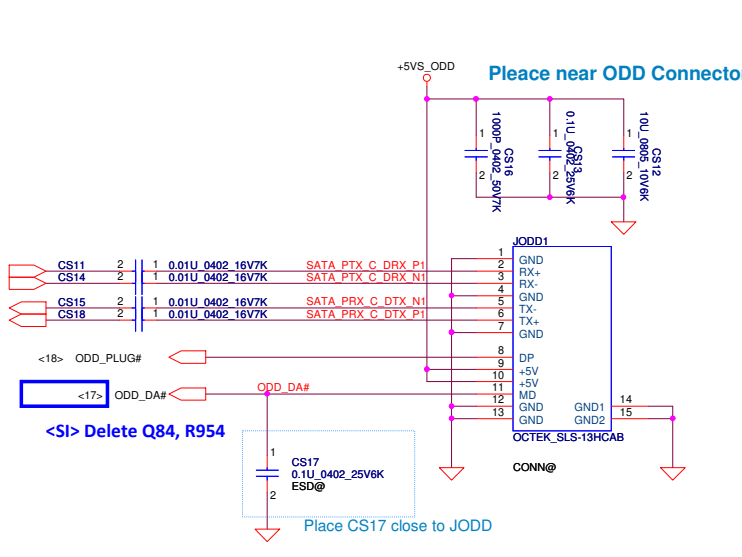
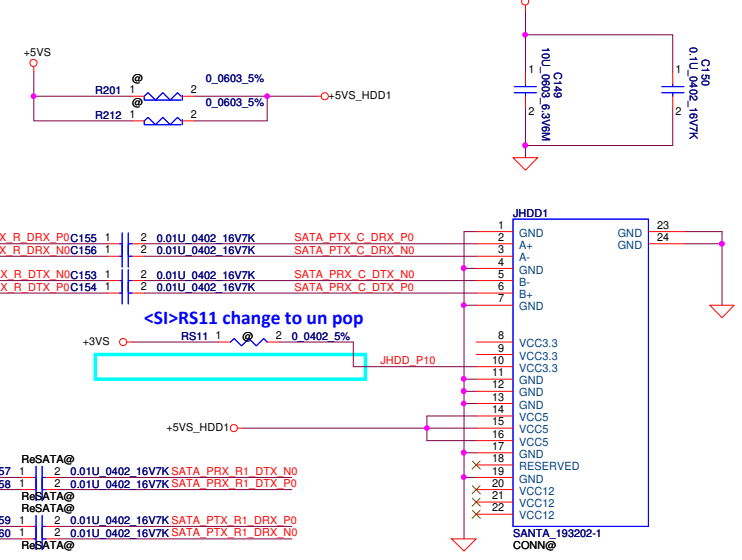
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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	WLAN
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Reserve SATA Redriver



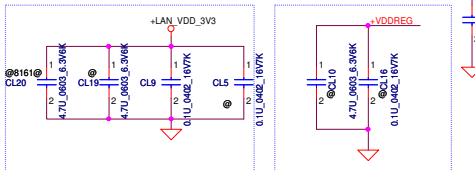
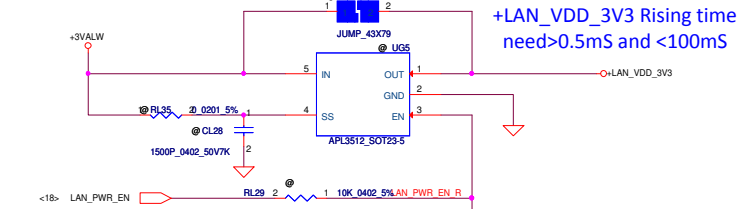
2.5" SATA HDD connector



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		LA-A999P		0.1	
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JHW1 need to short

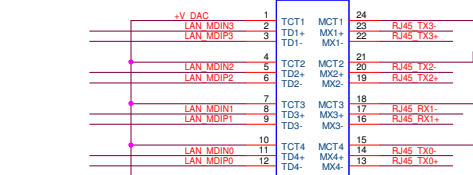
+LAN_VDD_3V3 Rising time need>0.5ms and <100ms



CL9 & CL5 close to UL1: Pin 11,32
CL19 close to UL1: Pin 32
CL20 close to UL1: Pin 11

CL10& CL16 close to UL1: Pin 23

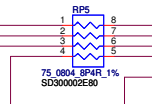
SP050005L00 Footprint



LAN_KO_LG2446S-1
SP050007M00
S XFORM_LG2446S-1 1001000BASE-TX LAN

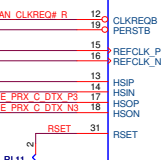
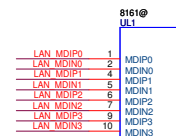
TS1 8166@
SP050003P00
S XFORM_NS892404 ETHERNET 10/100

(SP050003P00) 10/100 8166@
(SP050007M00) Giga 8161@

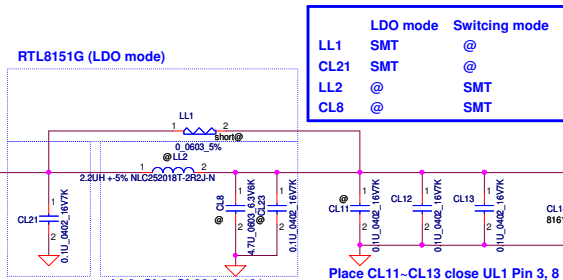


131127 SWAP Pin of DL1.2 & DL1.3 by layout requested

8151/8166 Co-Lay



(SA000063500) 10/100 8166@
(SA00005YT00) Giga 8151@



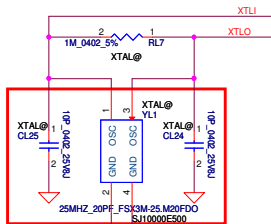
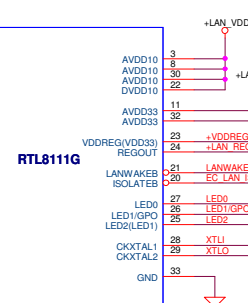
	LDO mode	Switching mode
LL1	SMT	@
CL21	SMT	@
LL2	@	SMT
CL8	@	SMT

CL14 & CL15 close UL1 Pin22
CL26 & CL27 close UL1 Pin30

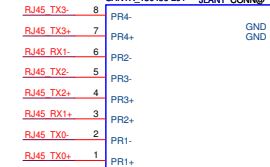
Place CL11-CL13 close UL1 Pin 3, 8, 22

LL2, CL8, CL23 for 8161
CL8 & CL18 close LL2

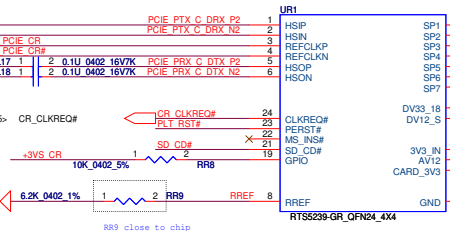
+LAN_VDD_3V3=40mil
+VDDREG=40mil
+LAN_REGOUT=60mil



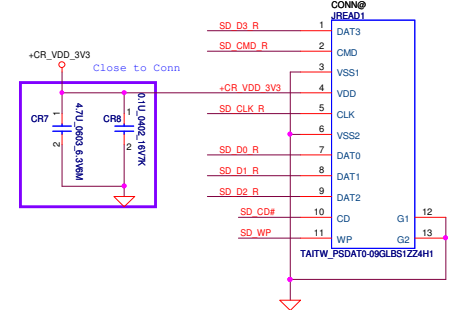
<1118>change to standard part.

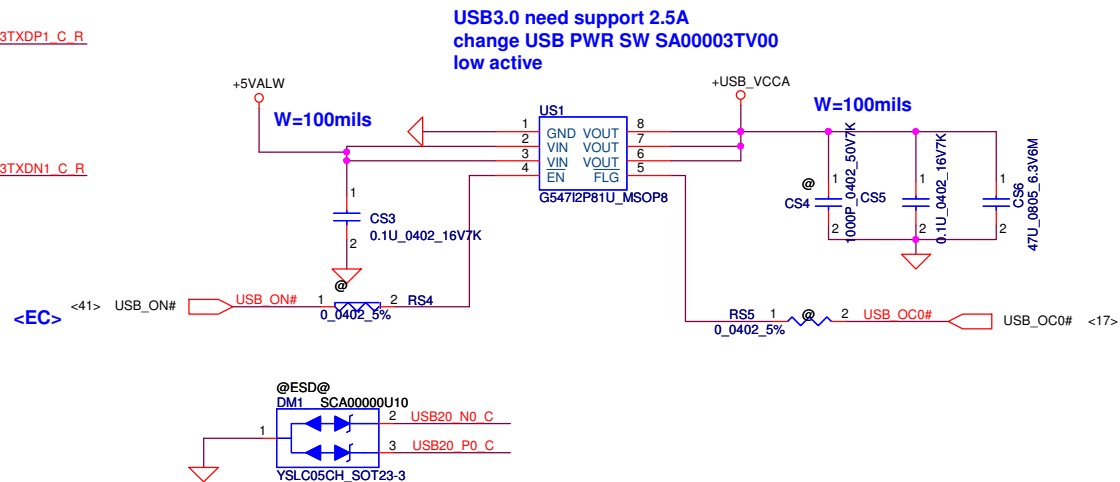
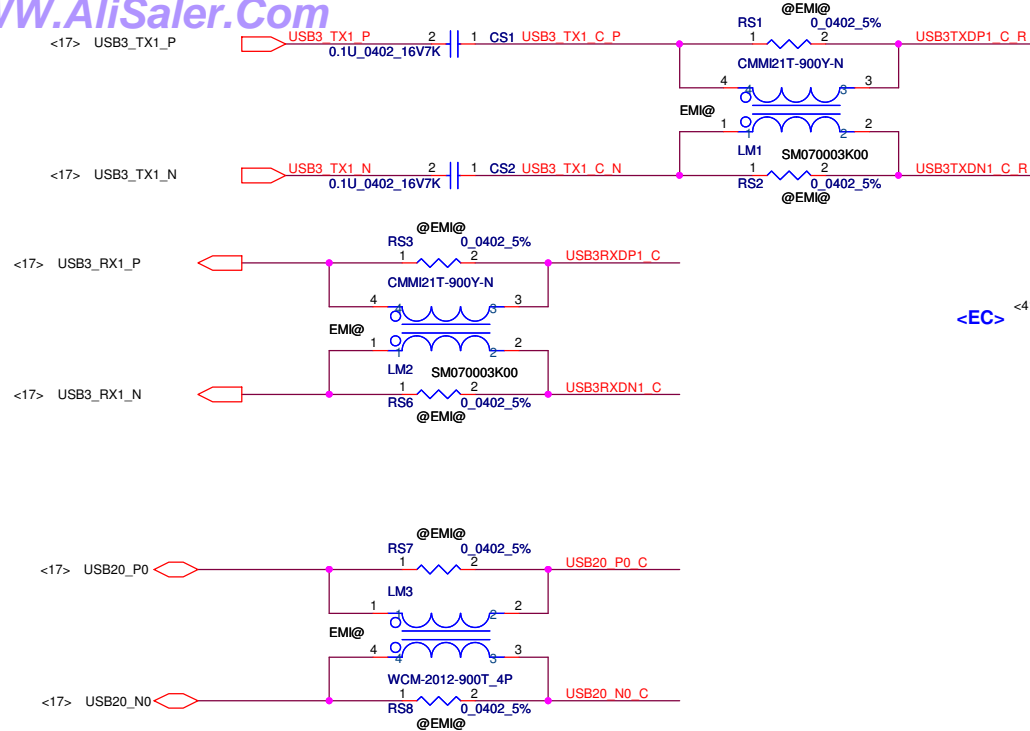


RTS5239

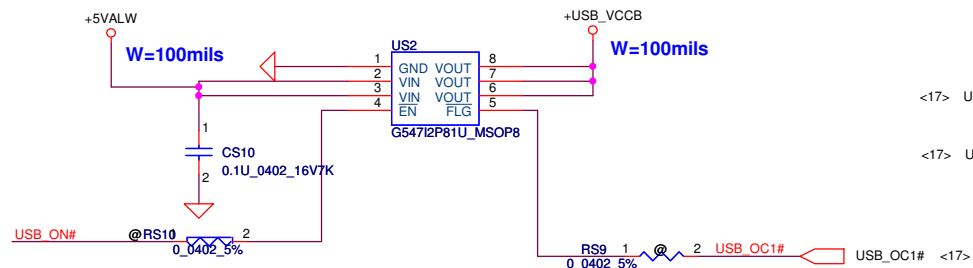


Card Reader Connector

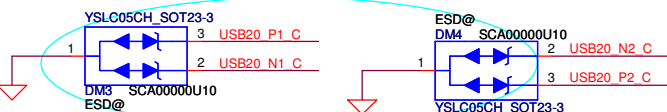




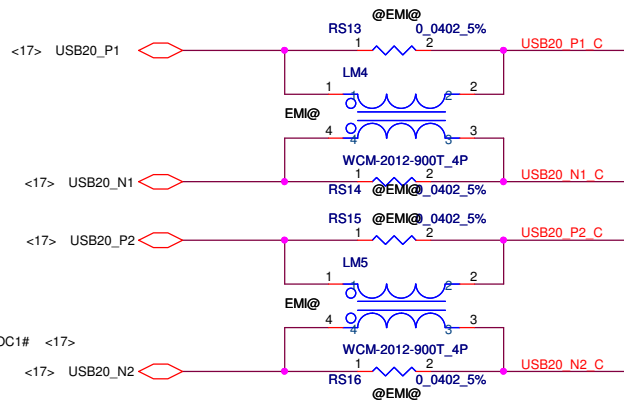
USB2.0 port x 2



131126 SWAP DM4.2 & DM4.3 by layout requested

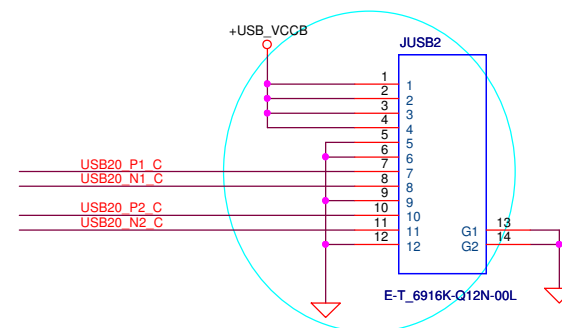


131129 change DM3 & DM4 to pop by ESD requested

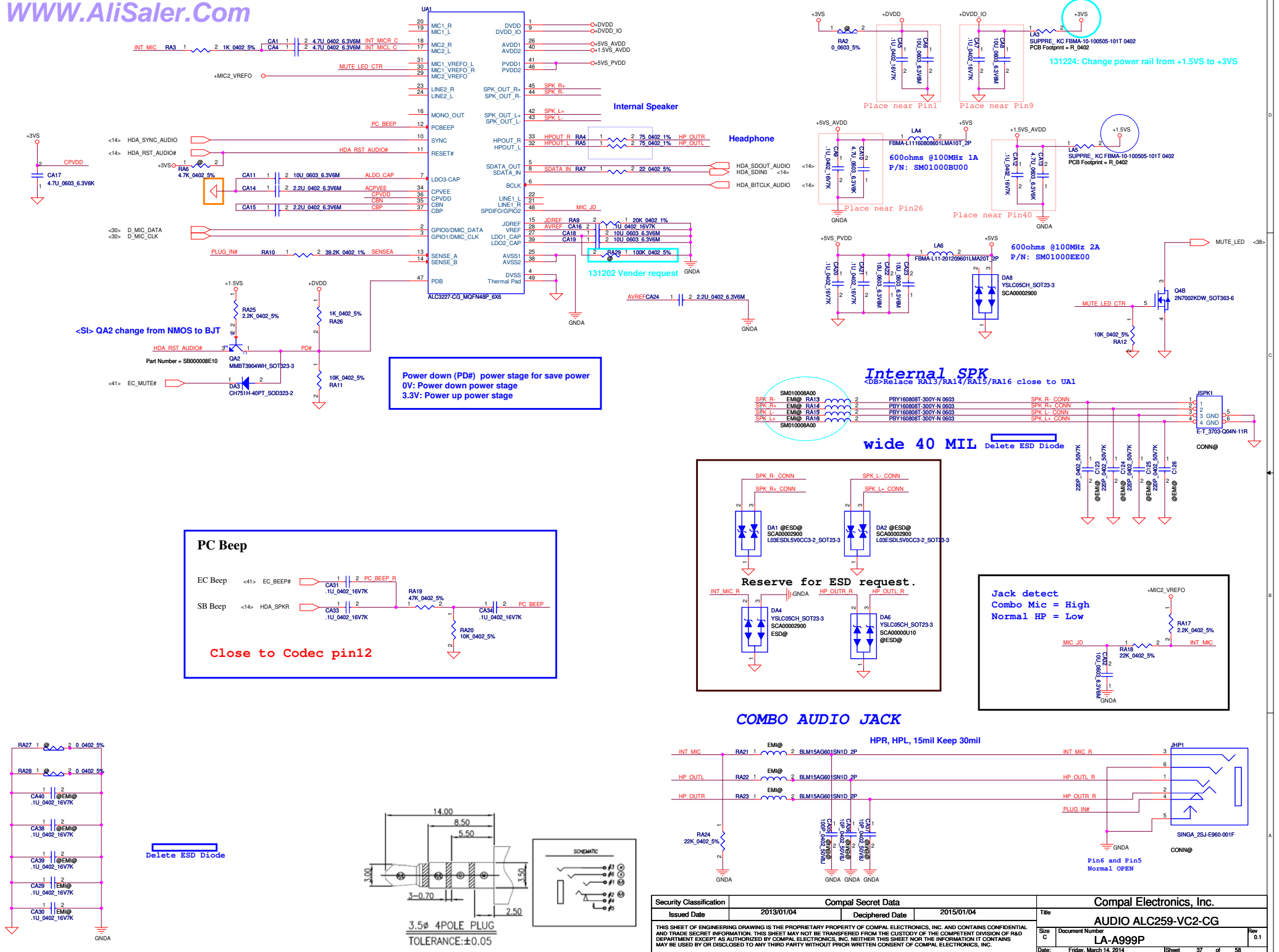


131203 SWAP pin of LM5 by layout requested

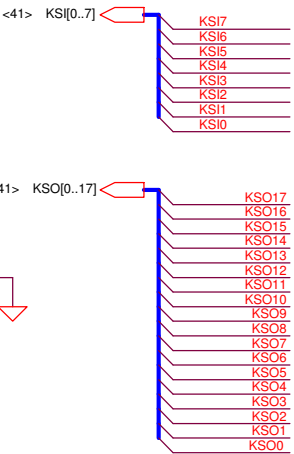
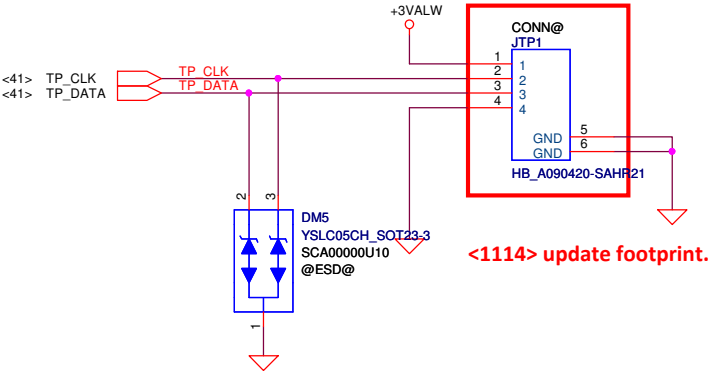
131126 reverse the JUSB2, follow haswell 14"



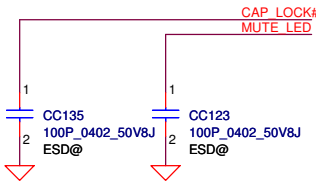
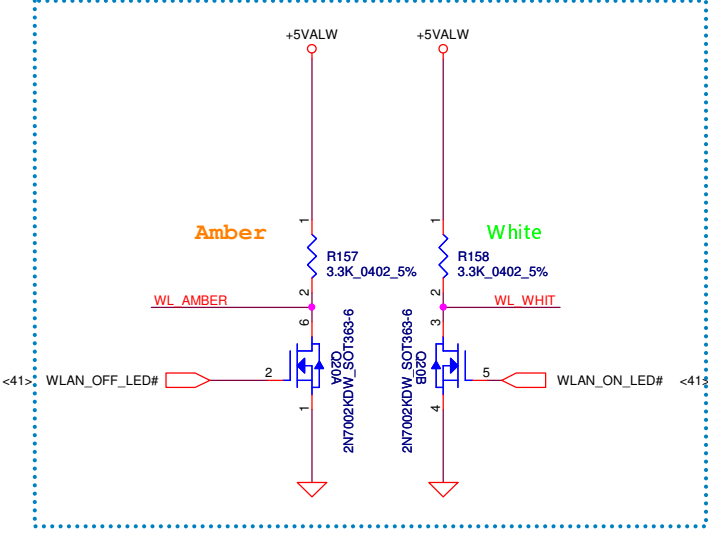
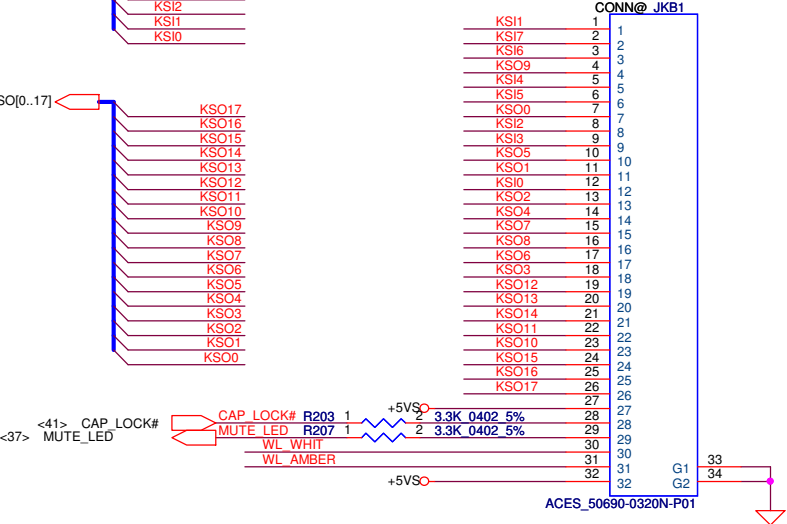
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Date				Friday, March 14, 2014				Sheet			
Friday, March 14, 2014				36				of			
36				58				Rev			
58				0.1							



Touch pad conn

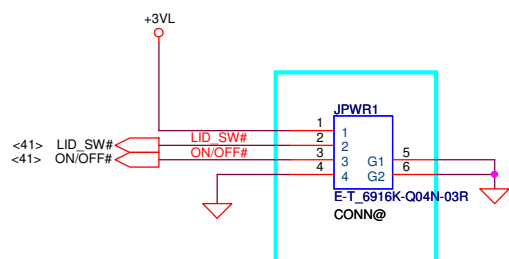


Keyboard conn



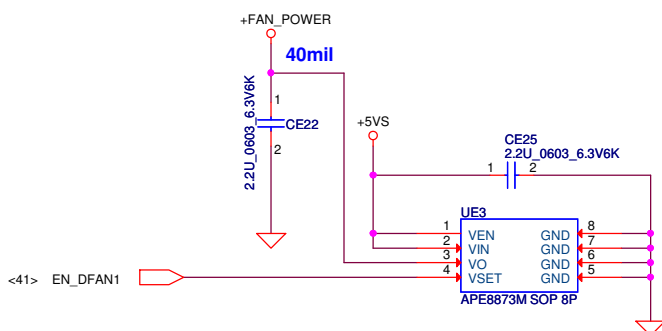
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Issued Date	2013/02/26	Deciphered Date	2015/07/08	Title	KB/TP
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Power Button Connector

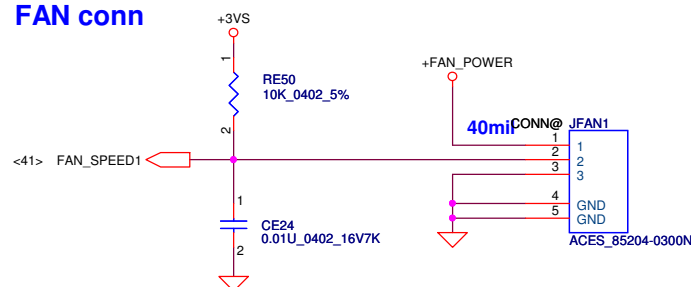


<1205> update footprint.

<SI> Del New Lid SW conn

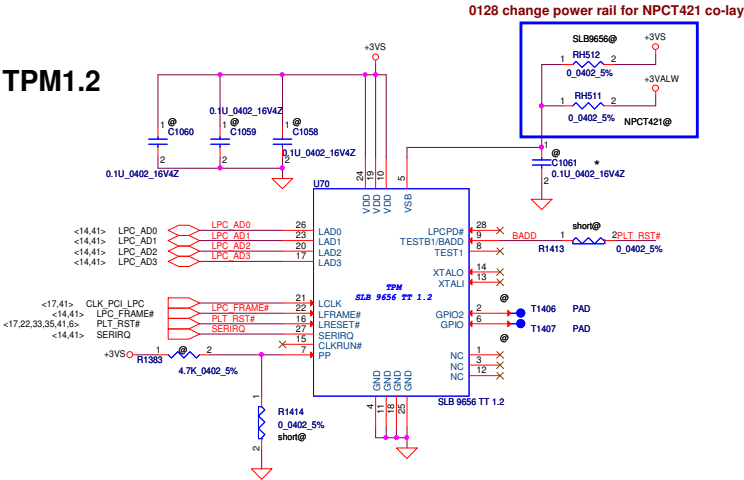


FAN conn

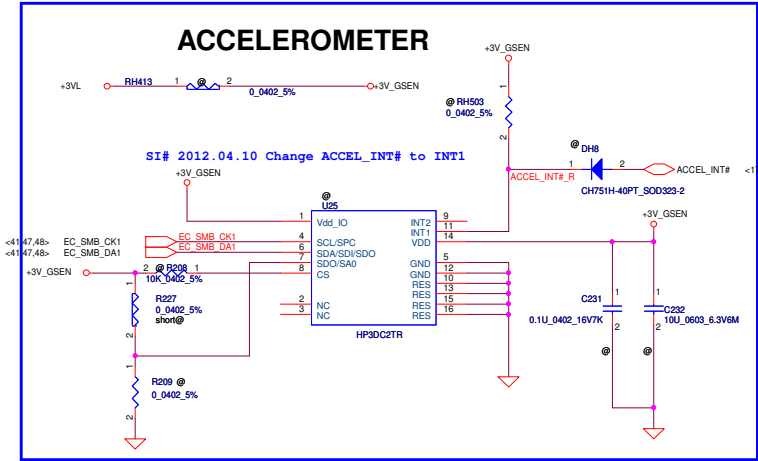


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				Date:	Friday, March 14, 2014
				Sheet	39 of 58

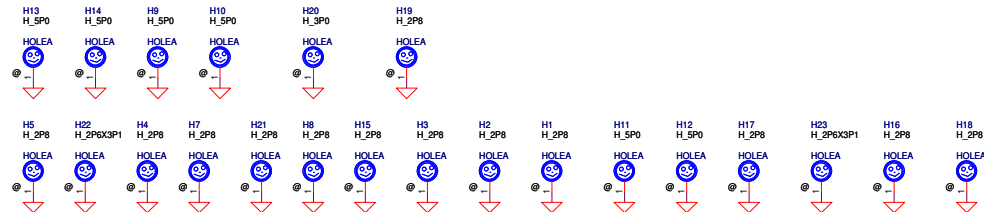
TPM1.2



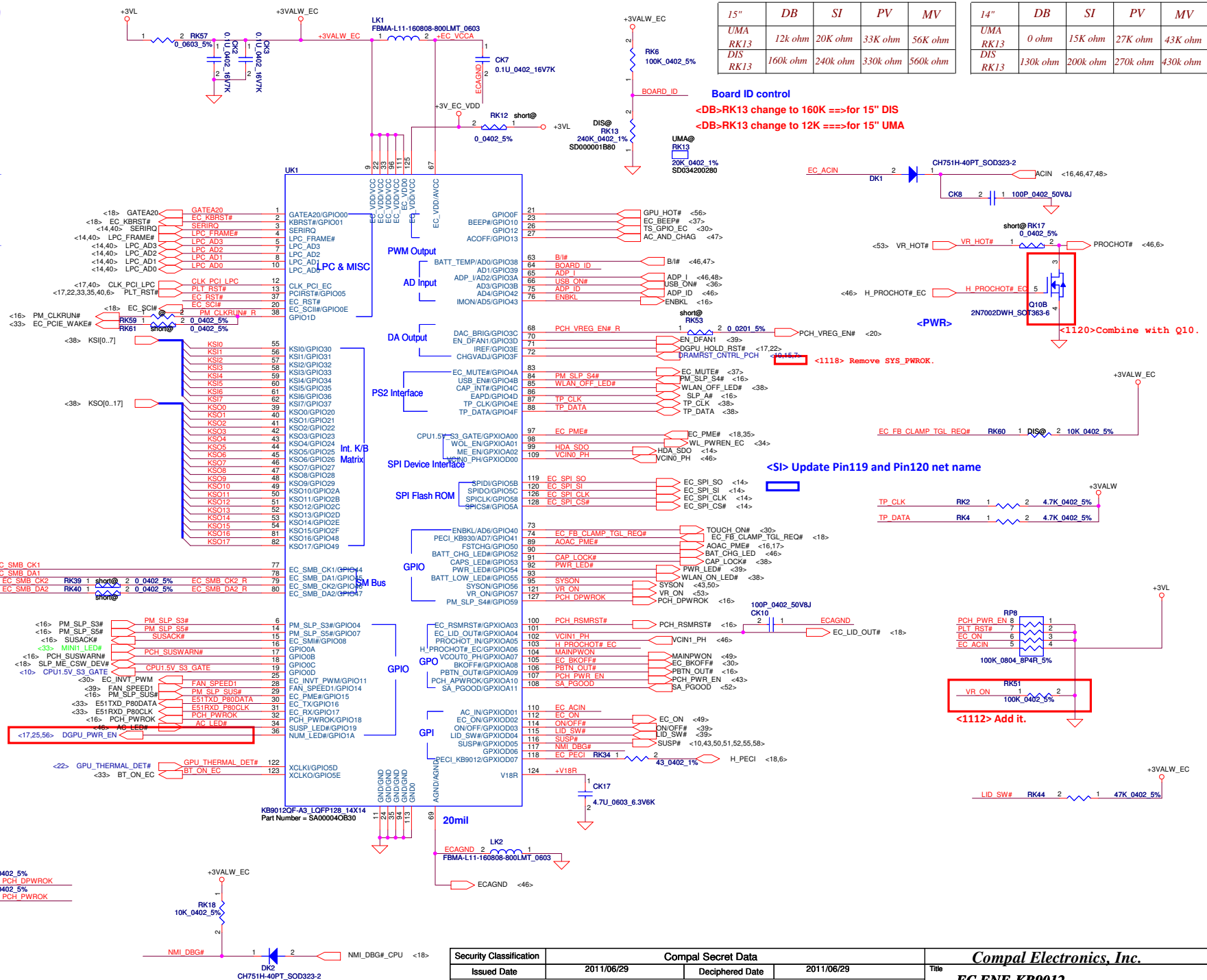
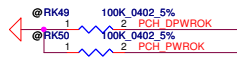
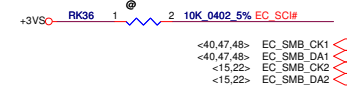
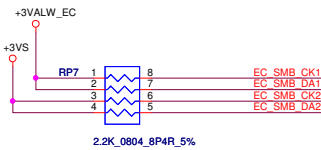
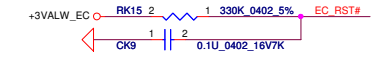
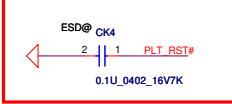
ACCELEROMETER



Screw Hole 131127 follow haswell 14"



PV# 2013.01.29 Add CK4 for ESD protection



15"	DB	SI	PV	MV
UMA	12k ohm	20K ohm	33K ohm	56K ohm
RK13				
DIS	160k ohm	240k ohm	330k ohm	560k ohm
RK13				

14"	DB	SI	PV	MV
UMA	0 ohm	15K ohm	27K ohm	43K ohm
RK13				
DIS	130k ohm	200k ohm	270k ohm	430k ohm
RK13				

Board ID control

<DB>RK13 change to 160K ==>for 15" DIS
<DB>RK13 change to 12K ==>for 15" UMA

<SI> Update Pin119 and Pin120 net name

<1112> Add it.

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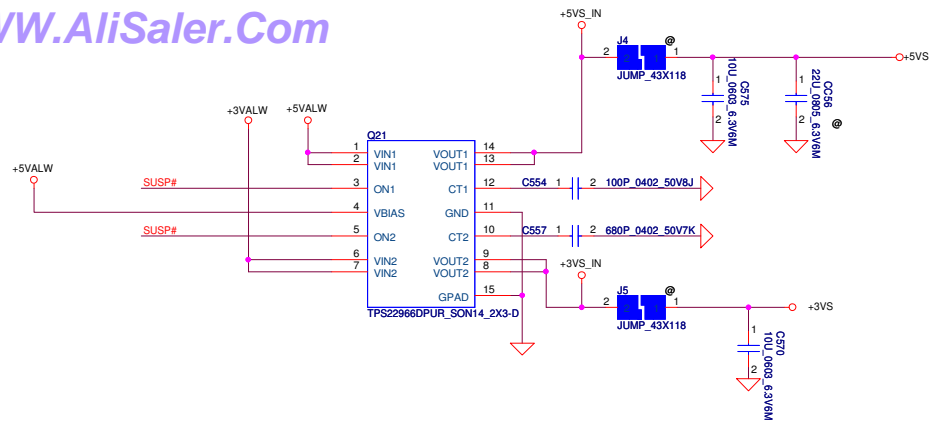
Green CLK no reserved.

BOM control

Platform	Silego P/N	Compal PN	25MHz(A)	32.768KHz	25MHz(B)	27MHz	8MHz	Remark
Intel CRV UMA	SLG3NB244VTR	SA000063300	1	1	1	X	X	GCLKUMA@
Intel CRV Dis	SLG3NB304VTR	SA000057I00	1	1	1	1	X	GCLKDIS@

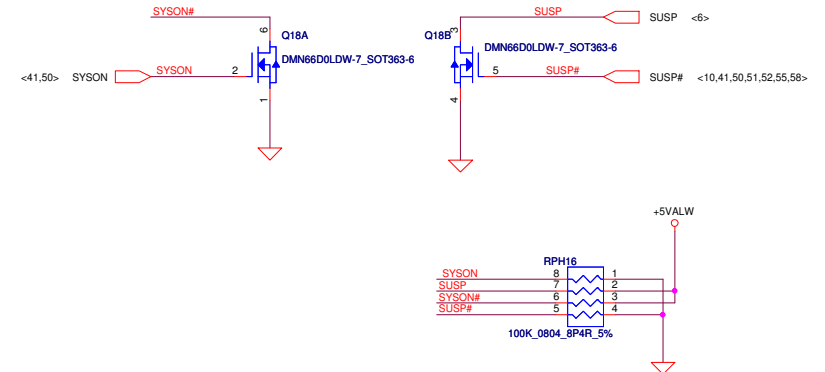
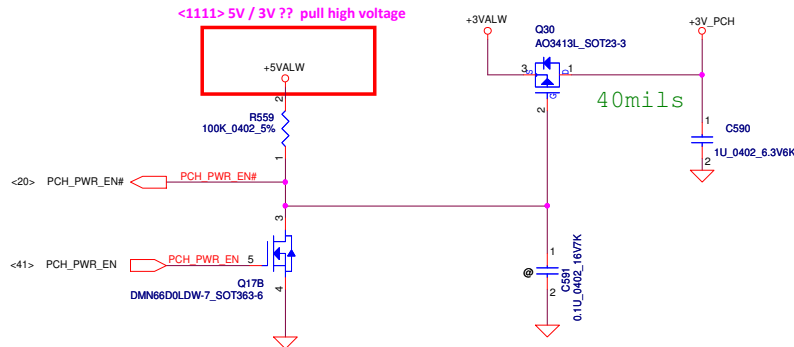
Base on A32 32.768KHz use 10ppm, G-CLK 25MHz X'TAL use 10ppm.

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				Document Number	
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+1.5V to +1.5VS

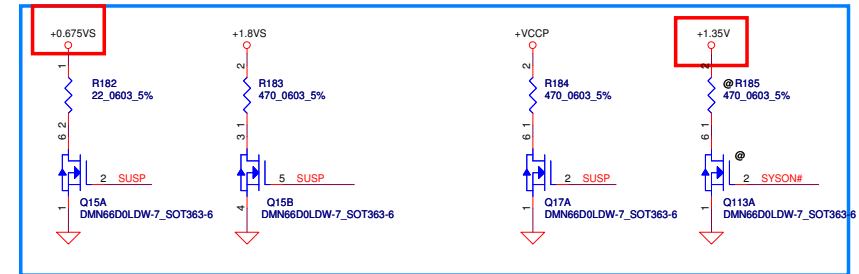
<1111> Remove +1.5VS DCDC.



AO4430L
VGS Max=+/- 20V
VGS(Th) max=2.5V

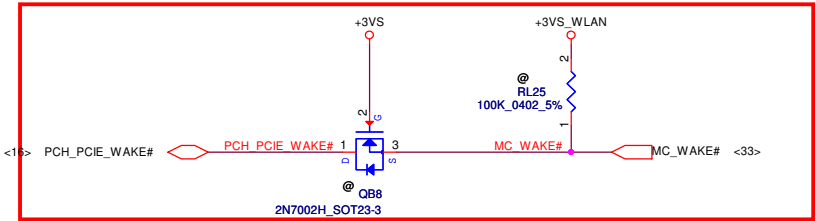
Rds Max=5.5m @VGS=10V
Rds Max=7.5m @VGS=4.5V

AO4430L
VGS Max=+/- 20V
VGS(Th) max=2.5V
Rds Max=5.5m @VGS=10V
Rds Max=7.5m @VGS=4.5V



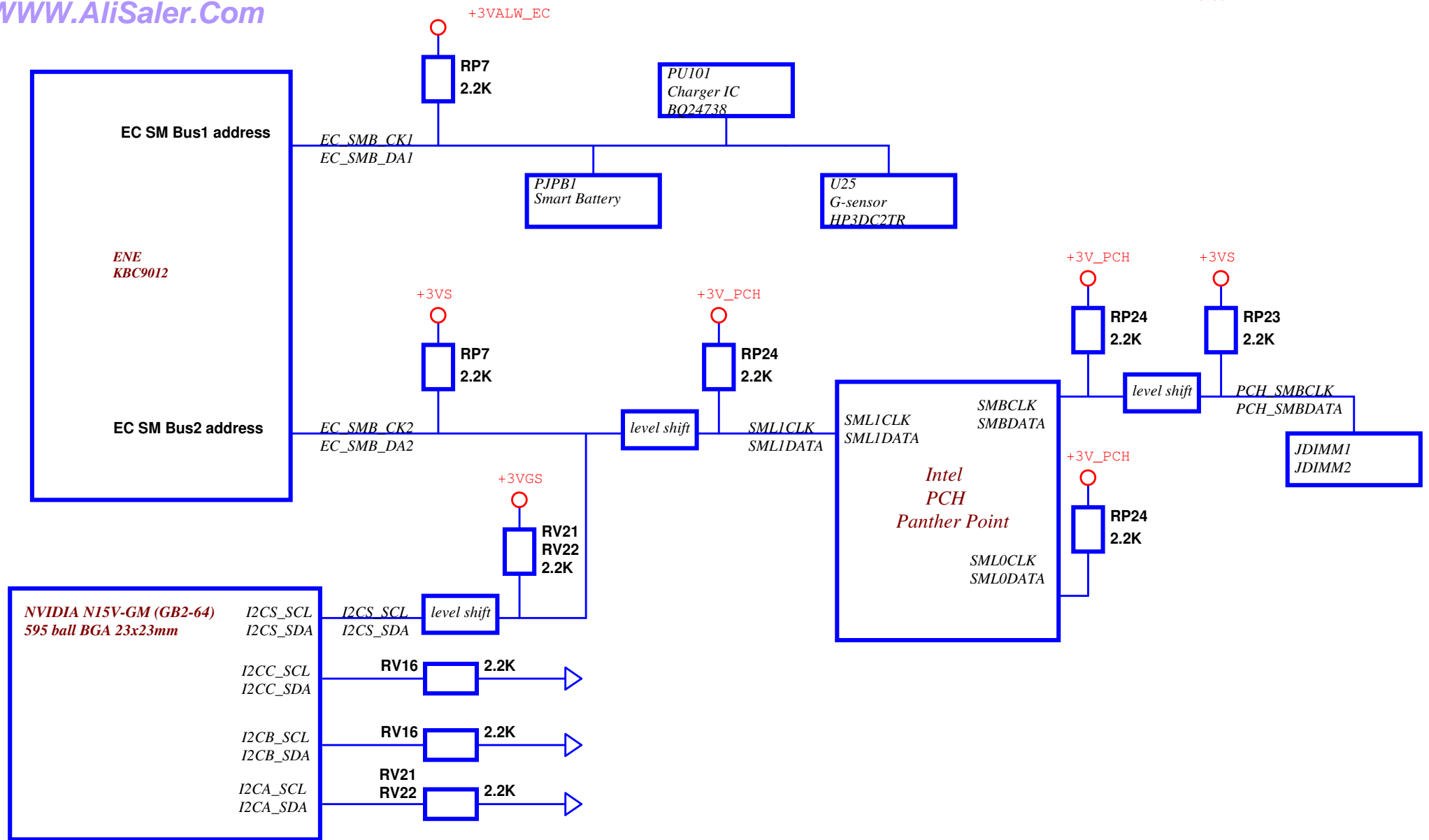
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Issued Date		2011/06/29		Deciphered Date		2011/06/29		Title			
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						Size		Document Number		Rev	
						Custom		LA-A999P		0.1	
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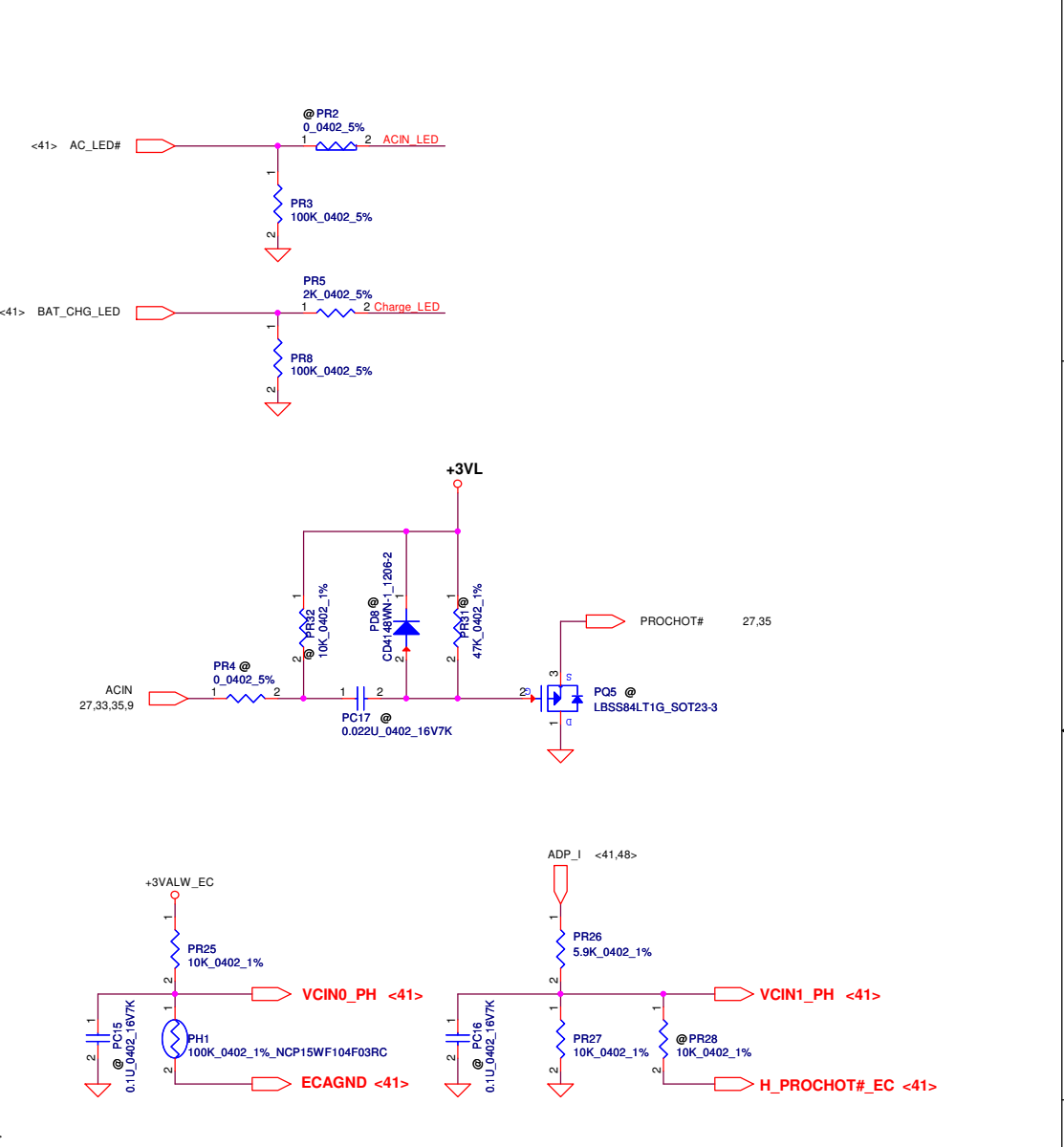
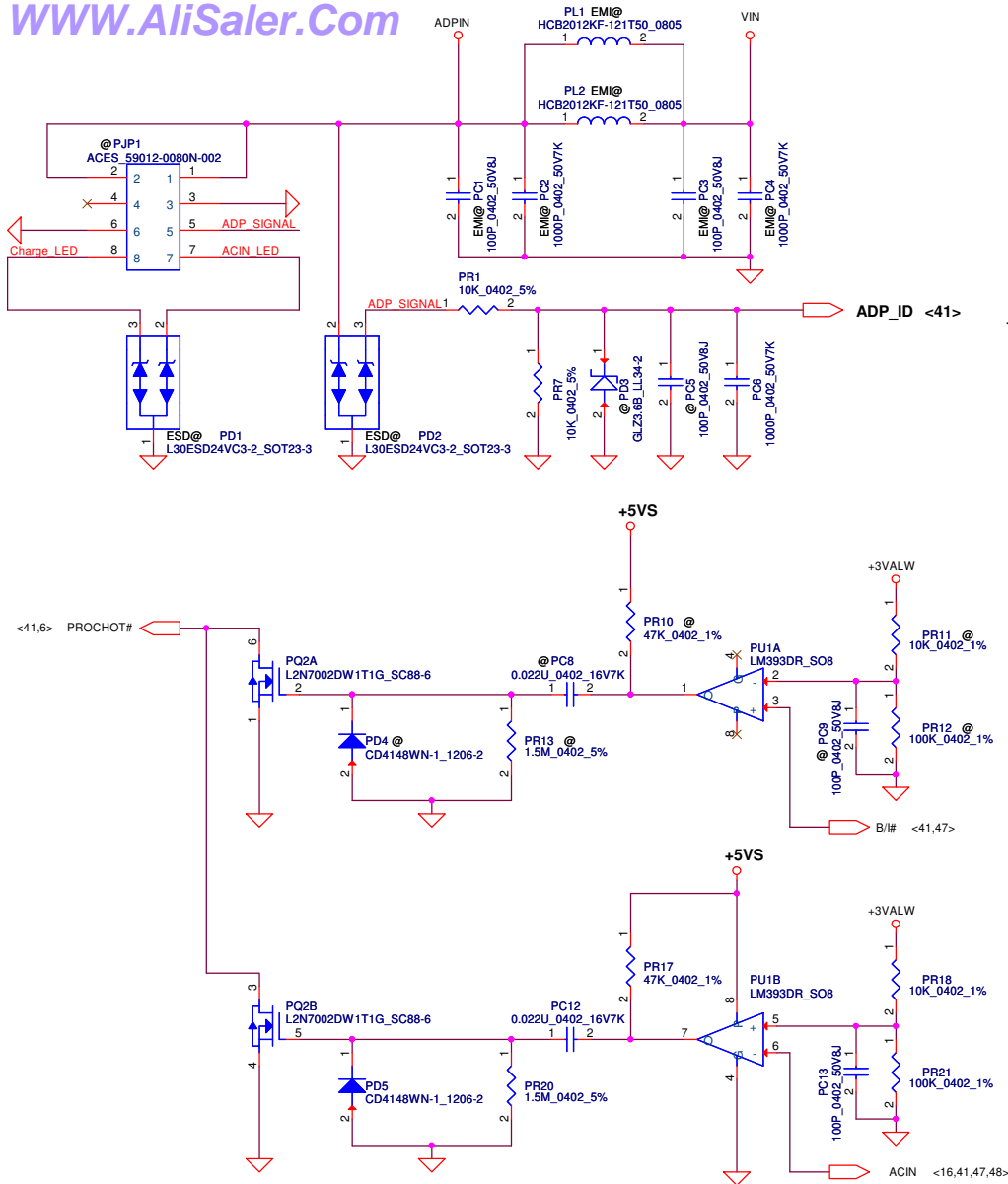
NGFF and WLAN



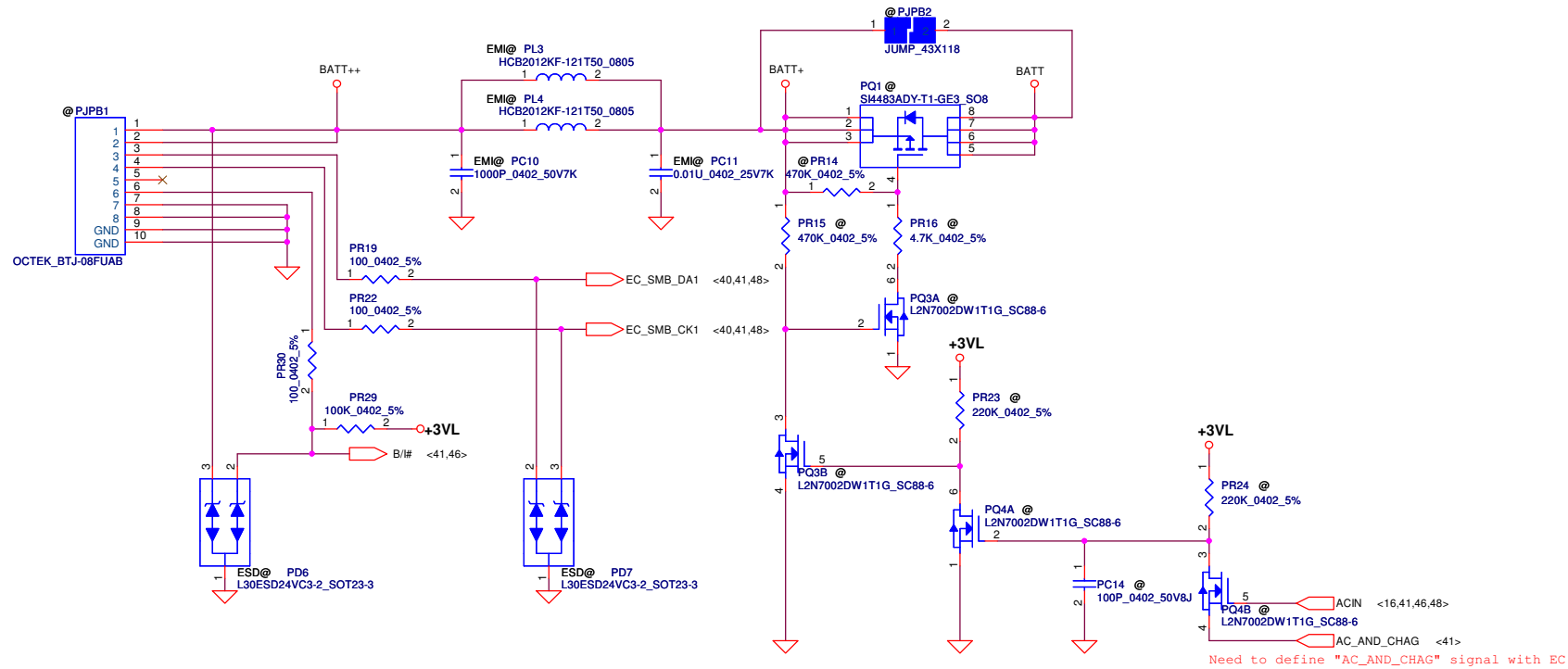
PV# 2013.01.23 Add QB8 abd RL25 to support OBFF
PV# 2013.02.22 Unpop QB4 and RL23 for not support OBFF

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				Custom LA-A999P	
				Date: Friday, March 14, 2014	
				Sheet 44 of 58	
				Rev 0.1	

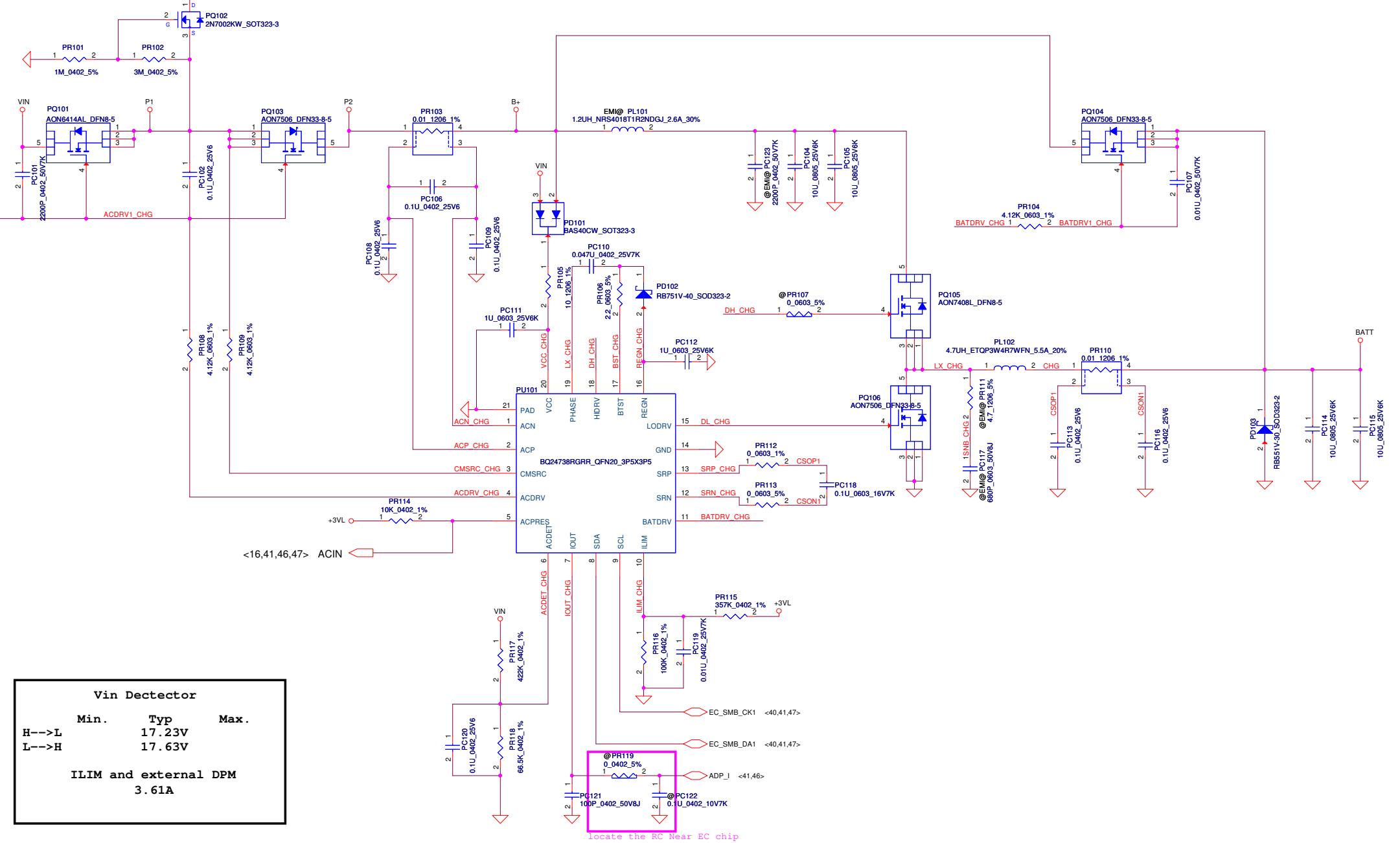


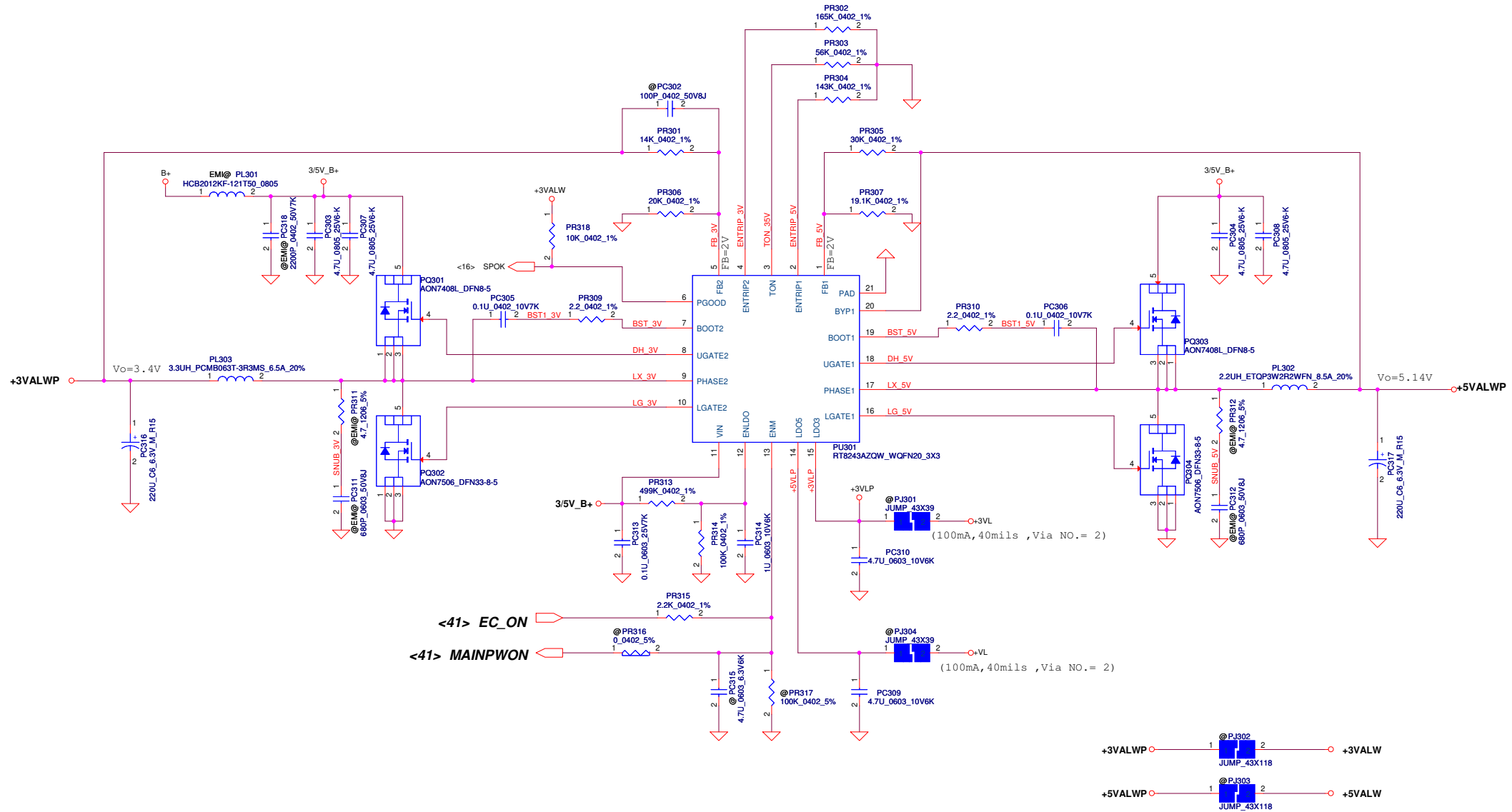


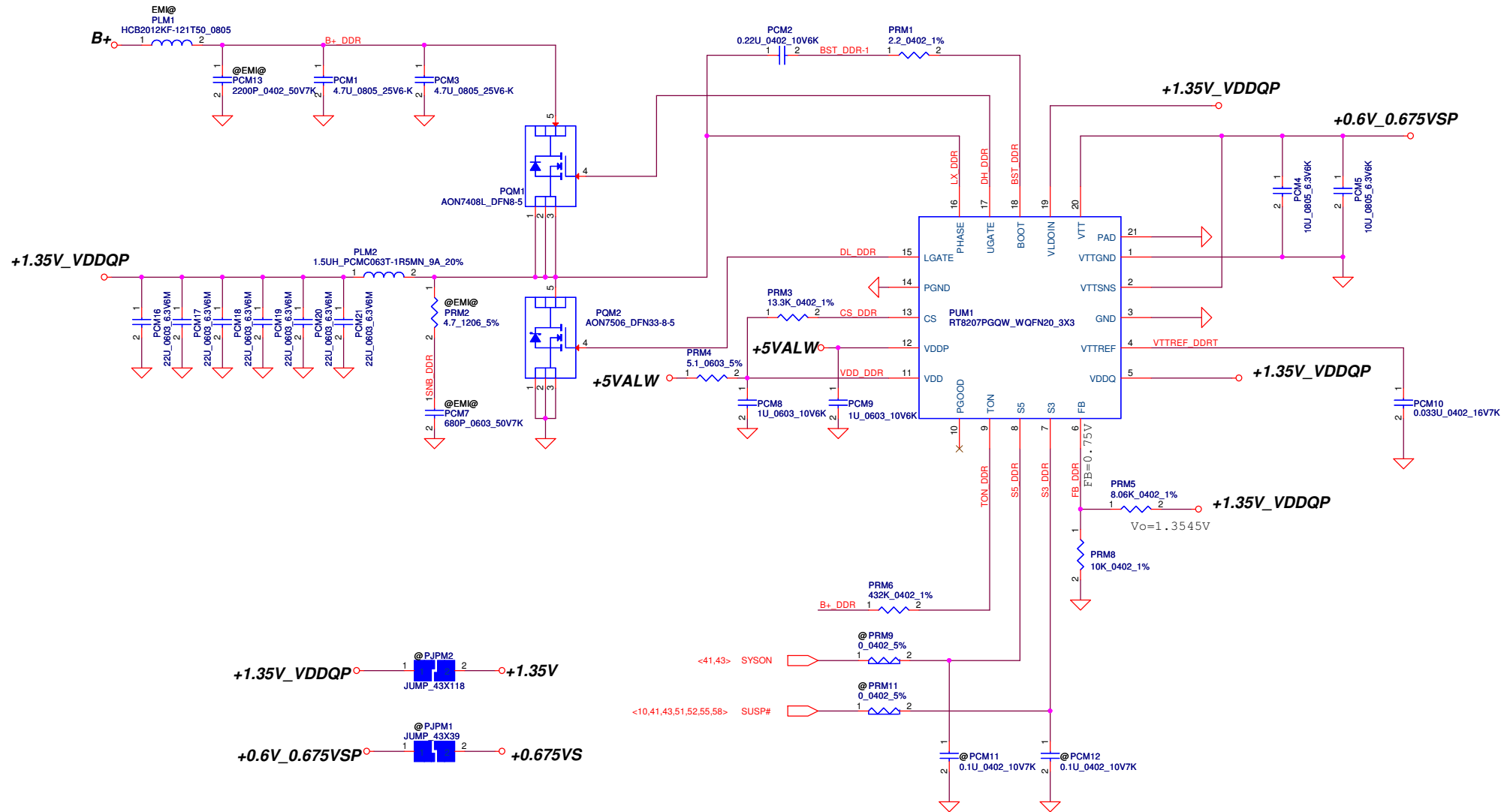
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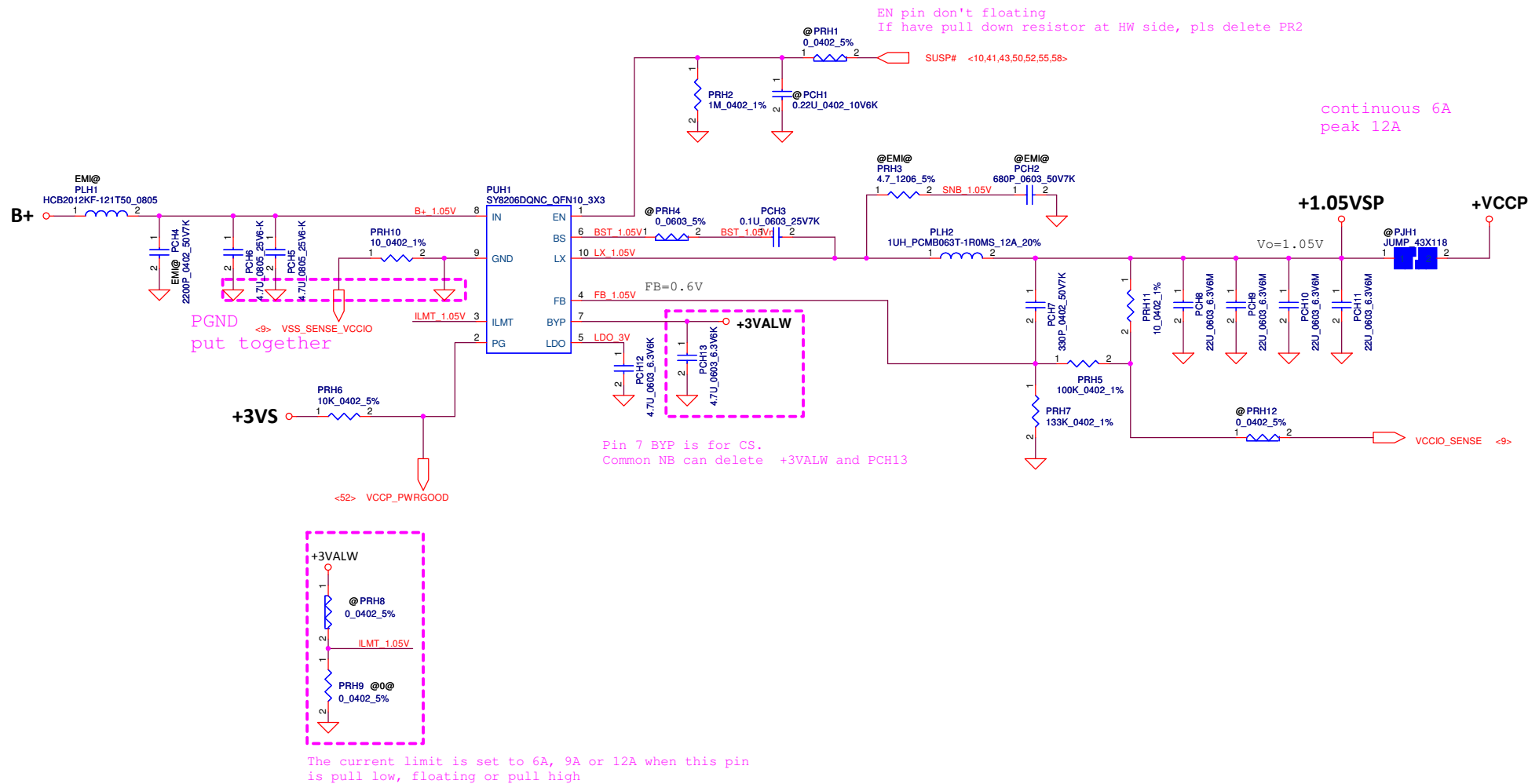
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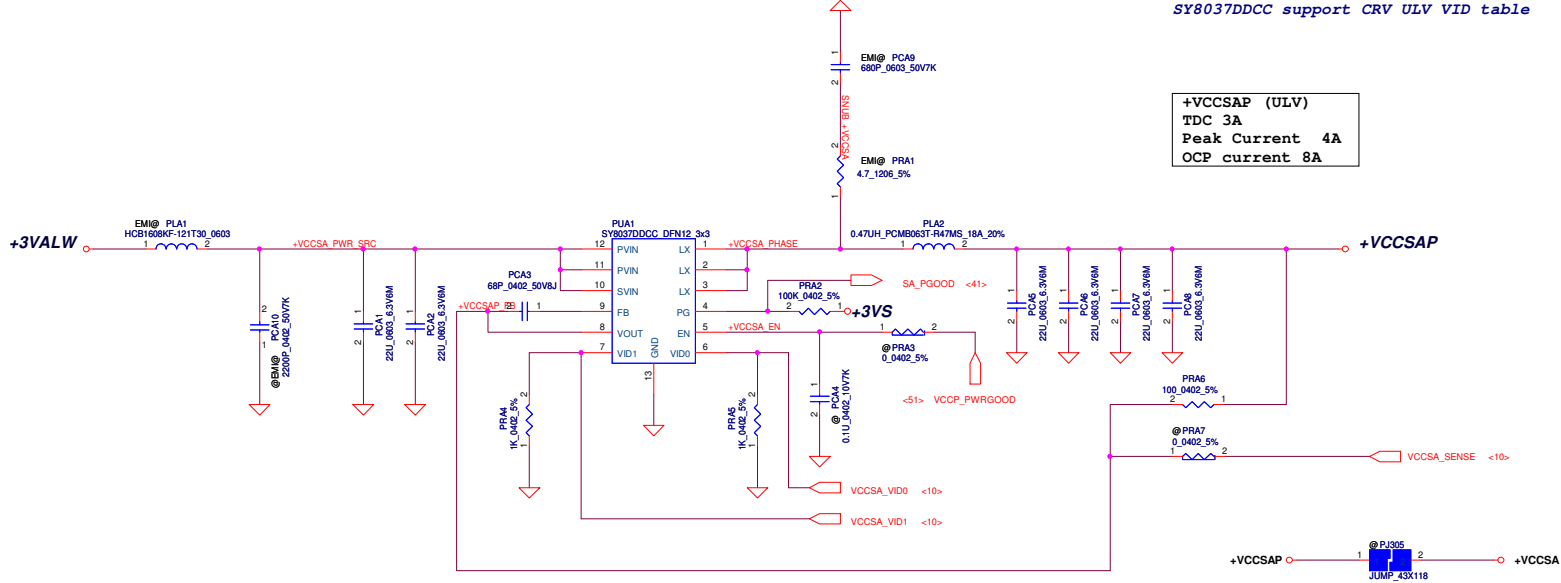




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Size	Document Number	Rev		0.2	
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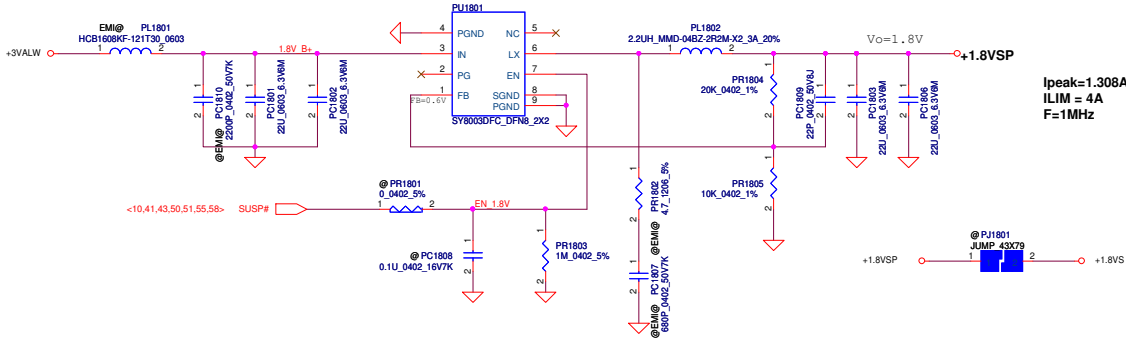


VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

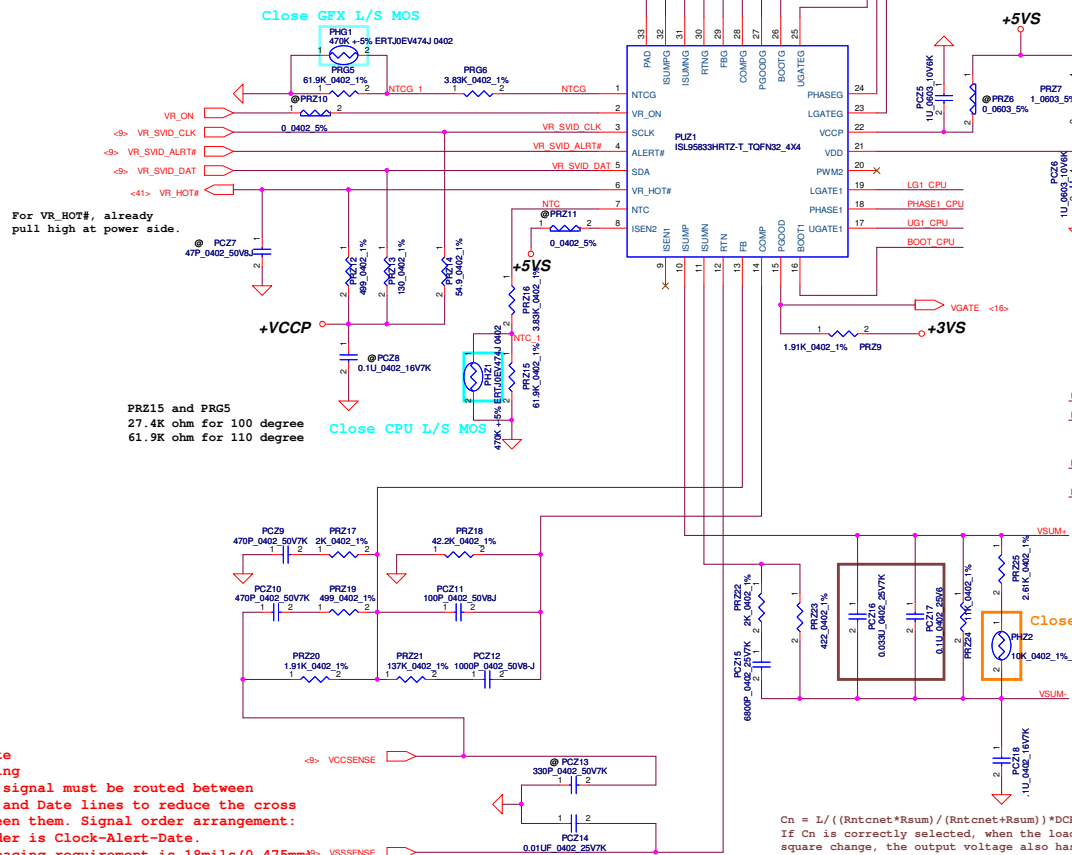
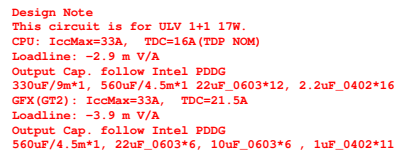
SY8037DDCC support CRV ULV VID table

+VCCSAP (ULV)
TDC 3A
Peak Current 4A
OCP current 8A

The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.

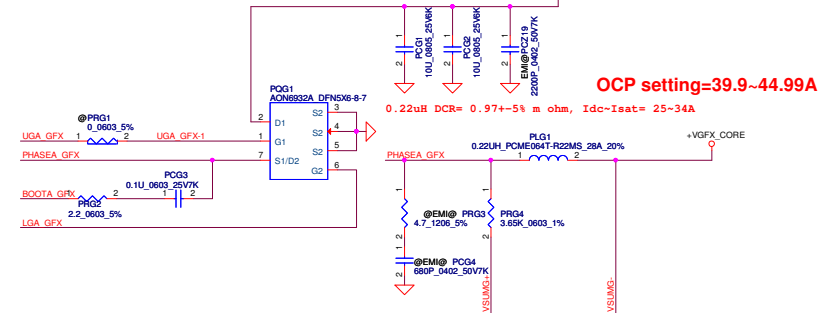


Ipeak=1.308A
ILIM = 4A
F=1MHz

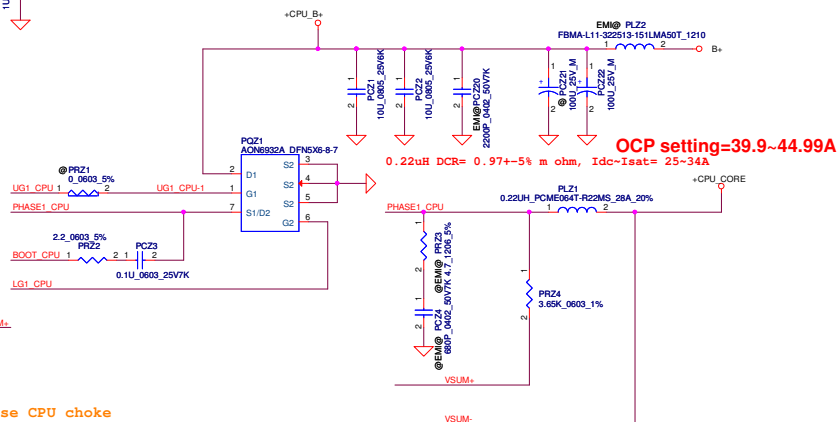


Layout Note
Reduce Acoustic Noise

1. The AL bulk capacitor of B+ should be very close to CPU_CORE MOSFET.
2. Input ceramic caps must place on symmetry same location on top side and bottom side.



VDD source use +5VS and PGOOD source use +
Please confirm power on and down sequence,
make sure VGATE after CPU_CORE on.

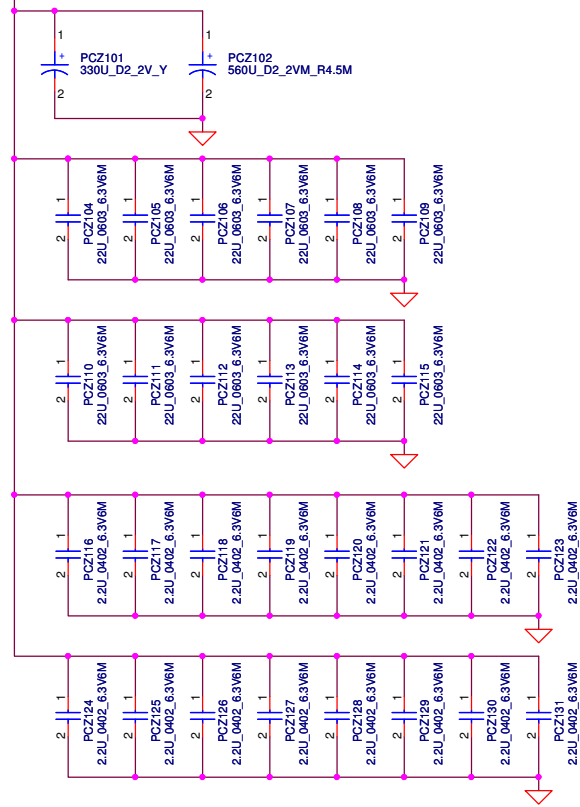

$$C_n = L / ((R_{ntcnet} * R_{sum}) / (R_{ntcnet} + R_{sum})) * DCR$$

If C_n is correctly selected, when the load current has a square change, the output voltage also has a square response

- Layout Note** VCCSENSE ☐
- SVID routing**
- Alert# signal must be routed between the Clock and Date lines to reduce the cross talk between them. Signal order arrangement: mobile order is Clock-Alert-Date.
 - SVID spacing requirement is 18mils(0.475mm); VSSSENSE ☐
 - Maximum total microstrip routing length of each SVID signal must not exceed 6000mils(152.4mm).
 - The SVID bus must be ground reference, It cannot be referenced to input (Vbat or 12V) power plans as they can couple noise into the SVID bus as power states change.
 - Avoid routing under noisy circuit, e.g. switch node , Gate driver, B+, Vin, high speed signal.
 - When SVID signal changes Layer, GND return path may be changed also. We need add GND via for GND reference.

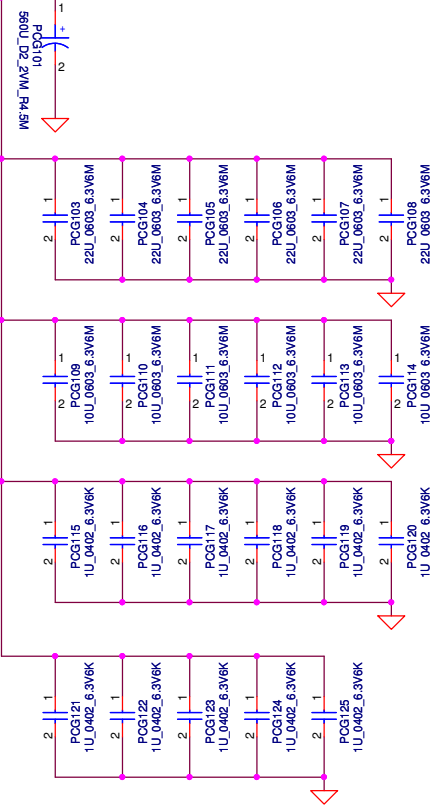
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+CPU_CORE



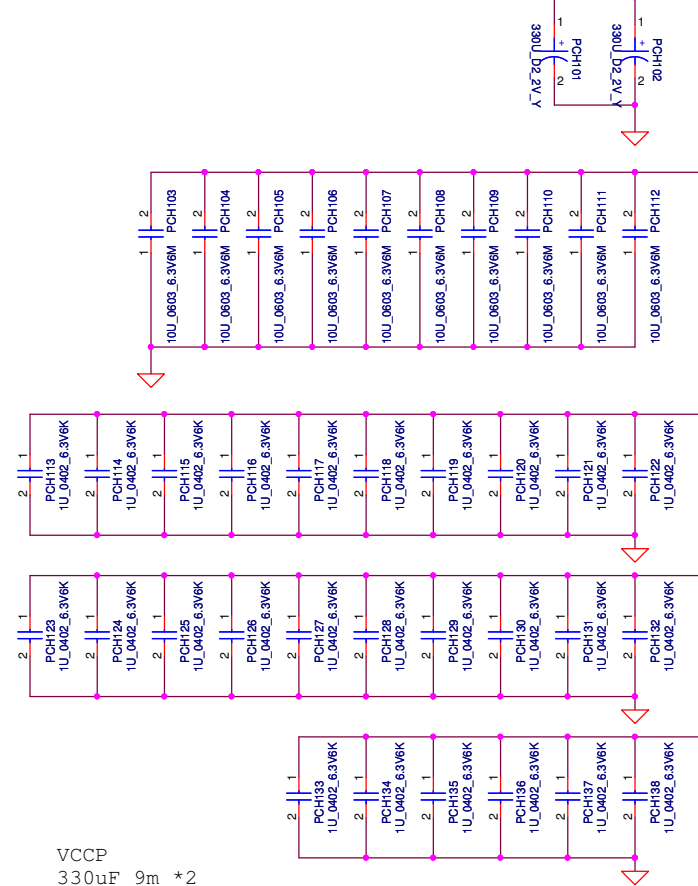
CPU_CORE
330uF 9m *1
560uF 4.5m *1
22uF 0603 *12
2.2uF 0402 *16

+VGFX_CORE



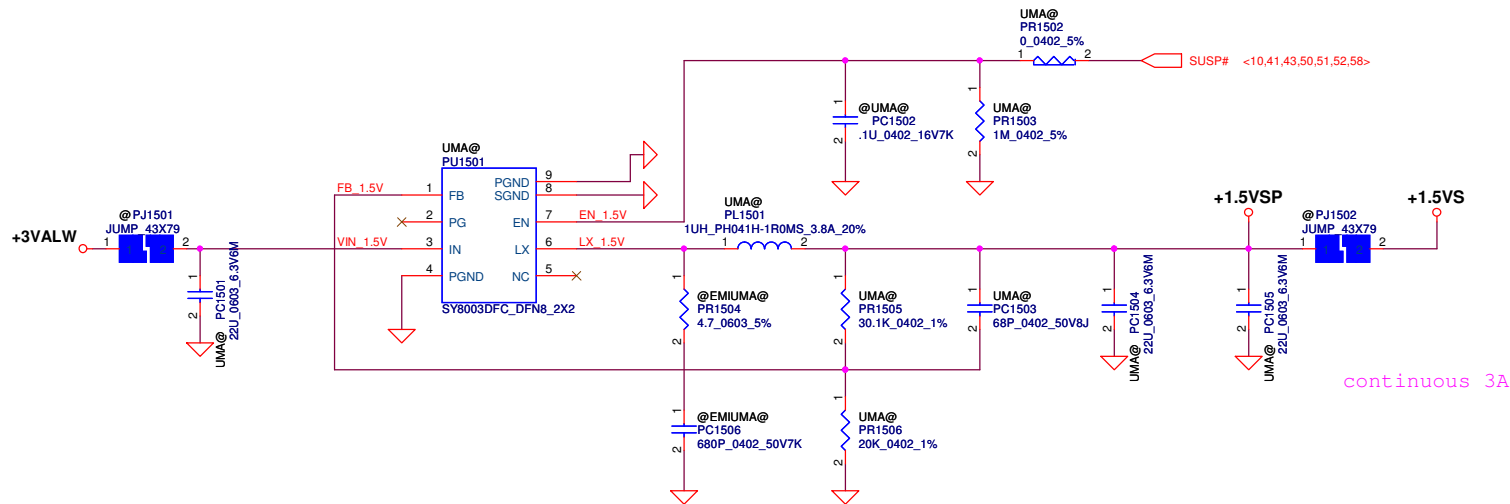
GFX_CORE
560uF 4.5m *1
22uF 0603 *6
10uF 0603 *6
1uF 0402 *11

+VCCP



VCCP
330uF 9m *2
10uF 0603 *10
1uF 0402 *26

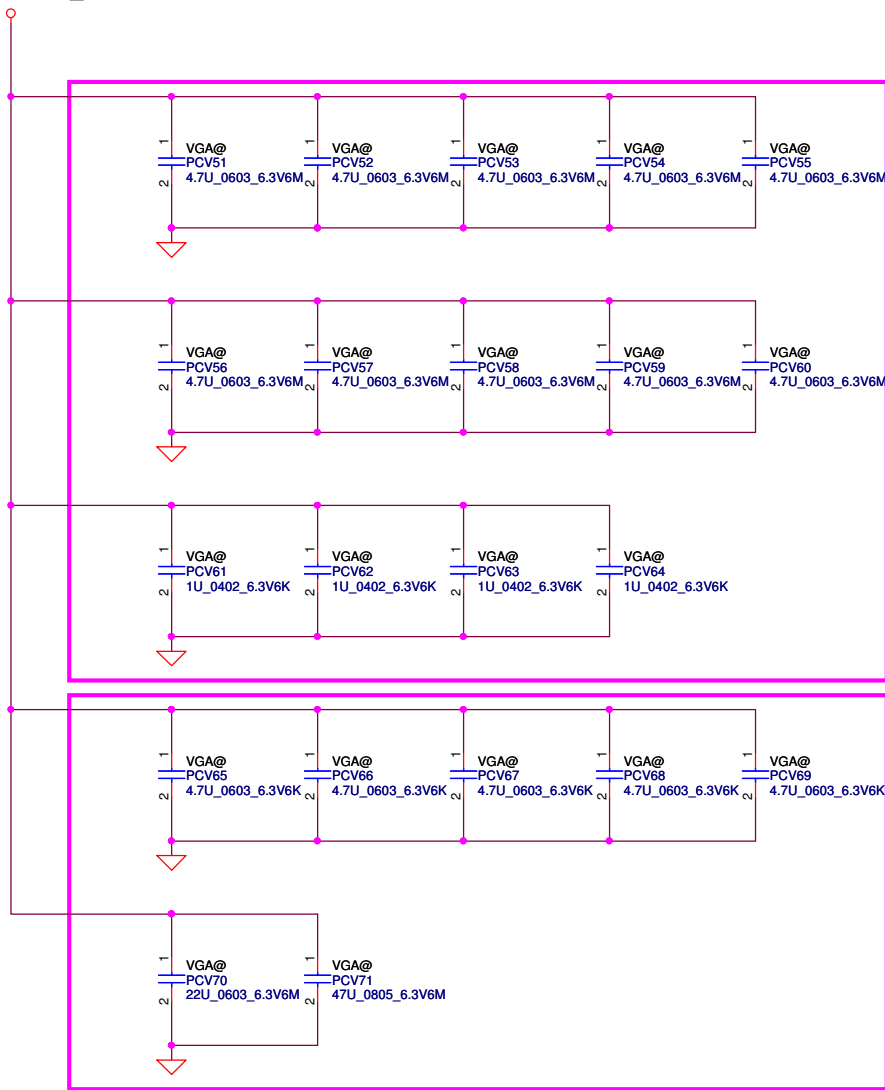
Security Classification		Compal Secret Data		Title	
Issued Date	2013/08/07	Deciphered Date	2016/08/06	PWR-CPU CORE DECOUPLING	
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				LA-A998P QFCAA	
				Date	Friday, March 14, 2014
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				Rev	0.2



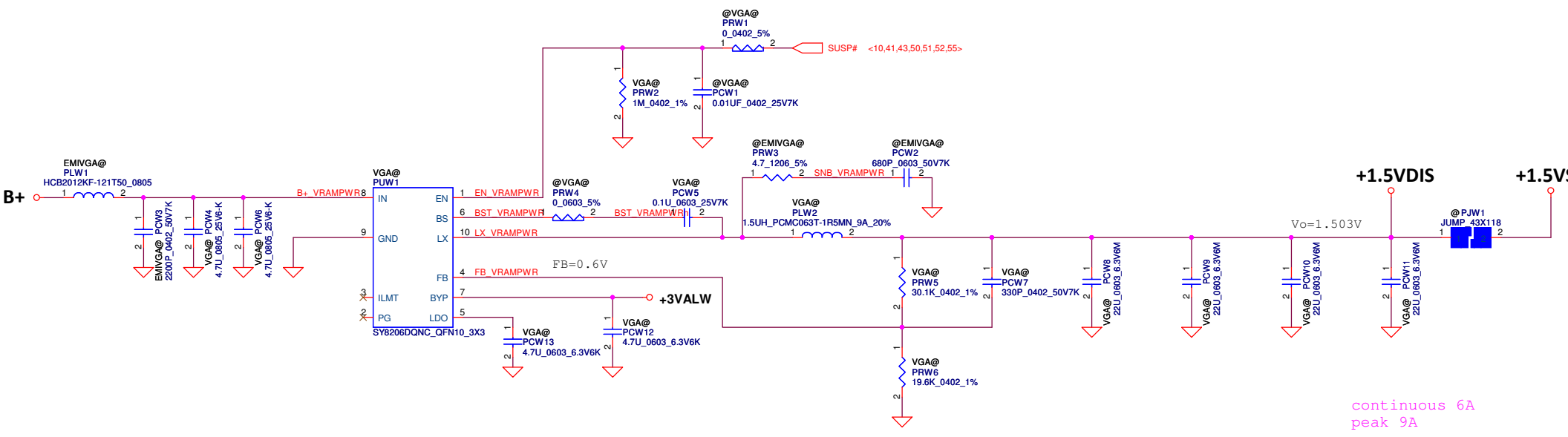
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